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A SPICE STUDY OF SILICON SENSOR STRIP NOISE ON LONG LADDERS

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by

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1 Introduction

1.1 Motivation

The International Linear Collider (ILC) is planned to be the world's largest, most powerful linear collider. It is designed to accelerate electrons and positrons to center of mass energies of up to 500 GeV, in order to better study whatever new phenomena may be discovered at the Large Hadron Collider. While a synchrotron (circular) accelerator, such as the LHC, can accelerate charged particles to extreme velocities far beyond the capability of a linear collider, it must use protons for its experiments – the energy loss due to synchrotron radiation, resulting from electrons moving in a circle at extreme speeds, makes using electrons infeasible. However, protons, being compound particles, are very "messy" when collided, resulting in large numbers of unwanted and uninteresting interactions between particles. This causes a great deal of interference, reducing the precision of any measurement. A linear collider, such as SLAC or the ILC, does not need to worry about synchrotron radiation, and can accelerate electrons and positrons freely. As a result, synchrotron colliders are often used for brute force work – for example, mapping out the energies at which a certain type of particle is likely to appear – while linear colliders are used for finer work, such as characterization of the particle in question.

The ILC is currently in the design and planning stages, with a highly tentative completion date sometime in the late 2010s. The particle beams will collide at a single point, where a state-of-the-art detector will record the results. Both detector designs being considered make extensive use of silicon microstrip sensors, in order to reconstruct the trajectories of the products from the collision. One of those proposed designs and the focus of this paper, the long ladder detector system, is a type of silicon sensor much longer and thinner than normal, and as such is being

proposed as a way to limit the material, electronic components, data overhead, and complexity associated with sensor readout, as well as increasing the precision of measurements. However, the precise long-ladder detector is a new development, and as a result a study of the system's performance and its noise is necessary – especially as the strip resistance noise is expected to grow nonlinearly with length, in the naïve approximation (see section 1.2.3). To this end, a physical study of this system was performed previously by Sean Crosby. I have continued his work by performing a SPICE study of this system, and the results of that study are the primary focus of this paper.

1.2 Background

1.2.1 Silicon Sensors

Silicon sensors are a popular choice for detecting ionizing particles and radiation. As a solid-state sensor, they can work at high speed, and with the modern photolithography used in the semiconductor industry, a sensor can be finely segmented into individual strips or pixels; this makes their positional measurements very precise.

A silicon detector can best be described as a silicon diode. In the case of the long-ladder detector, n-type silicon, silicon doped with electron donor elements, is used as the bulk of the detector. P-type silicon, or silicon doped with electron acceptor elements, is implanted in strips 7 μ m wide on the surface, with about 50 μ m between each strip. While these are quite ordinary dimensions for short-strip silicon detectors, the thing that makes the proposed long-ladder detector unique is its extraordinary length of up to one meter or more. A layer of aluminum is laid on top of the p-type implants, with a dielectric in between, to create a capacitance, and is read out by local microelectronics. The total length of the narrow strips makes Johnson noise a

much bigger problem for the long-ladder detector than a normal one, as shall be explained in the section 1.2.3.

By applying a positive potential to the underside, and connecting the p-type strips to ground via a large bias resistor, a reverse bias is created. This results in a diode effect, which only allows charge to flow in one direction, as well as what is known as a "depletion region," where charges, electrons and holes are swept out of the detector volume. When a particle passes through the detector at relativistic speeds, it ionizes the doped silicon, freeing thousands of electrons and creating equal numbers of holes in the depletion region. The holes collect on the p-type strips. Their flow is a current pulse that is then detected and read by the LSTFE-1 chip attached to the aluminum strips that are capacitively coupled to the p-type strips. Actual measurements are provided by comparing the amplifier readout to a pre-set threshold voltage, to distinguish a real pulse from the omnipresent noise fluctuations. A silicon-strip detector of any kind has hundreds of strips in parallel, and one can determine precisely where a particle hit by taking a weighted average over the charge deposited in the two or three neighboring strips, which collect the released charge. It is thus very important that noise be kept low, so that real pulses are distinguishable and their origin can be determined with accuracy.

However, silicon detectors also usually require cooling and they suffer from radiationinduced degradation problems, in addition to being much more expensive than older methods, such as cloud and wire chambers. It is hoped that the silicon detectors at the ILC will be able to get away with not needing an active cooling system – an objective that the long-ladder system, with its reduced number of electronic components, may be able to help to reach.

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1.2.2 An Explanation of the Long-Ladder Detector

The "long-ladder detector," so named because of its great strip length of up to a meter of more is being considered for service in the ILC because of just this fact. Its length reduces the number of readout amplifier chips (and associated electronics) necessary, and by extension reduces the cabling, heat, and data overhead from the detector system. This also results in less material between sensor arrays, which in turn results in better tracking and momentum measurements.

The ILC's beam is planned to cycle at 5 hertz (1 ms on, 199 ms off), and so to produce less heating from the electronics, it is proposed that they be switched on and off with the cycling of the beams. Since the electronics will be immersed in a magnetic field of five Tesla, the internal electronics will experience a periodic impulse as the current that powers the chips is switched on and off. This will result in the electrical equivalent of repeated blows with a hammer upon any and all electronics in the detector chamber. This is yet another benefit of the long ladder system – the reduction in readout electronics and current-conducting servicing will reduce the detrimental effects of this periodic Lorentz-force hammering, and generate less of a load on the power supplies.

On the flip side, the extraordinary length of this detector, combined with its unusually small strip width of 7 μ m, results in a correspondingly high resistance and capacitance, which itself leads to a significant amount of noise. The 80 cm long-ladder system proper is currently being modeled on a 128-strip silicon detector, using 4.75 cm strips, laid out in parallel, and daisy-chained together to form a single, unified strip about 62 cm long, with about ten grounded, unused strips in between each main strip to reduce crosstalk. This is where the "ladder" metaphor comes from: each strip is parallel to the next, each one forming a rung, or step, of the ladder.

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Each individual step is about 4.75 cm long, 7 μ m thick, with a resistance of 287 Ω and a capacitance of 5.2 pF. Measurements and calculations are taken in odd numbers of strips – 1, 3, 5, 7, 9, 11, and 13 – because it is more convenient to connect the strips to the electronics on the same side. When data at a larger or smaller length needed to be taken, strips can simply be included or excluded from the circuit. At 13 steps, the full ladder has a resistance of about 3.73 k Ω , and a capacitance of about 67.6 pF. Since, as can be seen in Eq. [2] in the next section, the noise is expected to grow nonlinearly with length, this would result in noise levels sufficient to compromise the integrity of the signal. It is expected that this will be the factor that limits the maximum ladder length as a function of the width of the strip.

1.2.3 Electronic Noise

Electronic noise is random fluctuations in an injected signal, such as that coming from a traversing subatomic particle. Noise reduces the quality of a signal significantly, and if the amount of noise is too high it becomes impossible to pick out anything of importance. The signal-to-noise ratio is thus an extremely important quantity in detector physics, as it is a direct measure of signal strength to noise strength. An S/N value of at least twelve is generally required to separate the signal from the noise.

Noise has a variety of causes. One obvious, and very important, source of noise is environmental radiation, such as light. In order to prevent signal corruption, sensitive electronics of any kind are always shielded against electromagnetic interference. Another important type of noise in detector physics is "shot" noise, a result of fluctuations in the leakage current that flows backwards through the diode, a result of quantum effects. A third type, called 1/f noise, arises from non-random fluctuations, such as when a charge carrier is trapped with various release lifetimes. Its density is inversely proportional to frequency, and as such is called low frequency noise. However, the dominating noise in the long-ladder detector is expected to be Johnson noise (or thermal noise), due to the detector strips' unusual length. Johnson noise is a result of thermal effects in the resistive elements of the detector and amplifier. In ideal form, this type of noise can be best summed up with the expression^[2]

$$V_{nR}^2 = 4k_B TRB$$
^[1]

where V_{nR} is the root-mean-square of the voltage noise, k_B is Boltzmann's constant, T is temperature, R is resistance, and B is the bandwidth in Hertz of an ideal band-pass filter.

Different types of noise must be combined and integrated over the frequency spectrum in order to estimate the noise from the sensor. Derivations in ^[1] show the noise for a sensor of characteristics I_d , R_b , R_s , and C, and amplifier of characteristics i_{na} , e_{na} , and A_f . The shaping factors F_i and F_v are of order one, and the time constant τ is a measure of pulse shaping. The resulting expression is

$$Q^{2} = F_{i}\tau(2eI_{d} + \frac{4kT}{R_{b}} + i_{na}^{2}) + \frac{F_{v}C^{2}}{\tau}(4kTR_{s} + e_{na}^{2}) + 4F_{v}A_{f}C^{2}$$
[2]

This yields a noise estimate in Coulombs squared. This approximation is rather naïve, however, as it assumes that the resistance and capacitance of a strip are lumped together into a single element when they are, in fact, distributed along its length.

 I_d is the leakage current through a biased sensor. It usually increases along with the bias voltage, leveling off at some characteristic level that for un-irradiated sensors is typically negligible relative to other sources. R_b is the value of the bias resistor connecting the implants to ground. In the "snake" apparatus it was chosen to be 40 M Ω , in order to keep its noise contribution low, rendering it largely negligible for our purposes. R_s is the ladder resistance of an individual strip, 287 Ω times the number of "rungs" in our case. *C* represents a combination of a

strip's capacitance to its nearest neighbors and contributions from the backplane. Neighboring strips were grounded, leaving this value well-defined as 1.1 pF/cm (5.2 pF per step).

Due to the length of the network for a large number of steps, and correspondingly large resistance and capacitance, the most important (squared) noise term is $4kTR_s \frac{F_v C^2}{\tau}$, corresponding to the Johnson noise of the strips feeding noise current into the strip capacitance. Its effect on long ladders is of particular importance, due to the nonlinear (three-halves power) dependence of noise on length. As can be seen, the strip resistance (R) is multiplied by the capacitance squared (C²). Since both are proportional to length, Q² ~ L³, or Q ~ L^{3/2}. This noise is expected to dominate for a sufficiently long ladder – hence the need to find out, using the SPICE model, whether or not this is the true behavior for a distributed system. Properly characterizing this nonlinear dependence on length in a SPICE program has been the focus of my project.

A breakdown and explanation of the noise components in this system can be found in section two.

1.3 The Project

In order to gain a greater understanding of the long-ladder detector system, I created a SPICE model whose noise output could be matched to that of the physical model, so that the nonlinear dependence of the noise on length could be better understood.

My predecessor, Sean Crosby, created the electronics setup and a physical model of the detector.^[3] However, when the results from the analytic model (Eq. [2]) were compared to measurements on the physical one, it became apparent that this naïve approximation was inadequate:



Figure 1: A comparison of Eq. [2] and physical measurements; note that the naïve approximation diverges at a large number of "steps," or as the length increases

As can be seen in figure 1, the Eq. [2] is clearly an inaccurate approximation, especially at large ladder lengths. The difficulty lies in the fact that the analytic model has a built-in assumption that the resistance and capacitance of the strips is in a lump, a single spot, as opposed to distributed evenly across the strip. Clearly, there was room for improvement in the analytical model. However, attempting to analytically model a distributed system is far from a simple task, which is why a SPICE study was recommended. The way SPICE is programmed makes modeling a distributed system, an essential feature of the setup, to a high degree of precision (<0.1%) relatively simple. Furthermore, an accurate SPICE model is much more efficient at predicting noise values and characteristics at larger loads than were initially analyzed – simulating a larger load is simply a matter of manipulating a GUI to attach more circuit elements.

In order to do this I have broken the physical model of the detector system into three parts, and created a simulation in SPICE. The charge injector system (to simulate a "hit" on the

detector strip) of the physical model is being directly simulated by a step-function voltage source and capacitor. The LSTFE-1 chip, which is being used for readout, is being simulated by a preamplifier, a differentiator (high-frequency band pass filter), and three integrators (lowfrequency band pass filters). The network of daisy-chained silicon sensor strips, the detector itself, has been simulated by an array of RC circuits, AC coupled to the rest of the system. Further details can be found in section 2; the results of this model and analysis thereof can be found in section 3.

2 Details of the SPICE Model

In SPICE, the circuit model for the 1-step setting on the detector is as follows:



Figure 2: The detector circuit diagram under the 1-step setting; the template from which this was designed was provided by Ned Spencer, the engineer who designed the LSTFE chip, and previous SPICE work done by Sean Crosby

This SPICE model has three essential parts: The charge injector, the LSTFE chip model, and the detector model. Contained in this section is a detailed explanation of each of these components. Section 3 contains details on the methods that were used to tune the SPICE model, and section 4 contains the results of this study. An explanation of SPICE commands can be found in the appendix.

2.1 The Charge Injector



Figure 3: The charge injector

The charge injector's purpose is to simulate a "hit" by a charged particle on the detector array, by implanting about 12500 electrons (2 fC) into the system. The V_Pulse element is a voltage source, set to the "pulse" setting, which allows SPICE to create square waves of various characteristics for the sake of simulation. The numbers in figure 3 associated with V_Pulse correspond to, in order, minimum voltage, maximum voltage, time delay between each pulse, rise time of the wave, fall time, time that pulse is at maximum voltage, and the period. All of these numbers were taken from the settings of the experimental setup.

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2.2 The Detector Model



Figure 4: The detector model, on the 1-step setting; note that the resistance (287 Ω) and capacitance (5.2 pF) of the strip has been divided into 8 RC circuits, to better simulate a distributed resistance and capacitance

The detector model is meant to simulate the detector service board in the physical setup. The actual, physical detector strips are a system of resistances and capacitances distributed continuously across the strip, a fact that the analytical model (Eq. [2]) failed to take into account. In order to simulate this in the SPICE model, we divided the resistance (287 Ω) and capacitance (5.2 pF) of each strip into eight RC circuits. Testing with the 13-step setting (which had the greatest sensitivity to this division) revealed that further division yielded only small improvements in accuracy, with the difference between an eight-fold division and a sixteen-fold one being <0.1% of the total noise. However, the above figure is not of the 13-step setting, but of

the 1-step setting; the size of the 13-step setting, at $8 \times 13 = 104$ RC circuits, would make it invisible on this page.

The C_AC_couple element is, as the name suggests, an AC coupling capacitor, placed in the physical model to ensure that no DC voltage crosses into the chip. R_big is a bias resistor. I_Noise_Probe is a 1 amp (AC) current source, and serves mainly as a bookkeeping element for LTSPICE's noise probe function. It has little effect on the model as a whole.

2.3 The LSTFE Chip Model



Figure 5: The LSTFE chip model; the preamplifier is in the upper left, the differentiator is on the center-left, and the integrators are everything else; measurements were taken between R_AMP2 and C_PASS2, corresponding to the shaper output

The LSTFE model is composed of three parts: the preamplifier, the differentiator, and the three integrators. The preamplifier is composed of the voltage-controlled voltage source E1 and the feedback resistor/capacitor R_P and C_P. The voltage-controlled voltage sources, in terms of the SPICE model, act primarily to give gain, and to invert the voltage vs. time curve. The

differentiator is composed of the VCVS E3, as well as the RC circuit elements of C_D and R_D. It acts as a high-pass filter, as part of the process to shape the injected square wave into a Gaussian-like wave. The integrators, composed of E2, E4, E5, and their attendant RC circuits, act as low-pass filters in order to further shape the wave. All measurements, physical and SPICE, were taken at the "output" of the LSTFE chip, which in the SPICE model corresponds to the node connecting R_AMP2 and C_PASS2.

The LSTFE model was the major element used to tune to SPICE model. Details can be found in the next section.

3 Tuning the SPICE model

The original SPICE model, as shown in figure 2, produced the following noise curve:





The original SPICE model, which was later used as a template for adjustments, was created with the assistance of engineer Ned Spencer, almost entirely as-is. The only tuning necessary was to split each detector step into eight, to better simulate a distributed RC circuit, and to adjust the resistors attached to the integrator units (R_I1, R_I2, R_AMP2), in order to adjust the peaking time to better match experimental data. However, as can be seen above, even after the template was properly adjusted the SPICE model did not give an accurate simulation of the noise, and various methods were used to try to account for this gap.

The first method was the "parasitic capacitance" method, which introduced parallel capacitors to ground in between each step in the detector unit of the SPICE model. It was

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believed that there might be some unaccounted-for capacitance on the physical setup, as a result of the wiring, causing crosstalk between steps and increasing the noise. Due to both inadequate results and the inherent difficulty in determining the physical value of this capacitance, this concept was eventually dropped.

The second idea was motivated by the recognition that the SPICE model did not include noise contributions contributed by the amplifier itself. The first attempt to address this involved using SPICE's "TEMP" function to increase the temperature of the entire model, and as an extension increase the noise. However, it was eventually decided that this was non-physical, and the idea was dropped. The method that was eventually favored is called the "ideal noise source." The ideal noise source is a resistor, placed at the input of the chip model, and made large or small enough to have no impact on the model's voltage vs. time behavior. It is then given a temperature, and the simulation is run. The result is an increase in the noise of the model, with no effect on the peaking time or gain. The temperature, and thus the degree of noise contributed by the ideal noise source, was tuned to match the observed behavior of the LSTFE chip (see section 3.6).

The ideal noise source provided a better approximation of the noise arising from the amplifier itself than the other methods, especially at a large number of steps. At this point, it was decided to further tune the model. This was done in two ways: first, the settings of the preamplifier were adjusted, both to stabilize the gain and to make it better match that of the physical model. Second, the RC circuit array was replaced by a single capacitor, in order to verify the sensitivity of the model to the capacitor-only load (for which we had data), and to use this to choose an appropriate temperature.

The actual noise values, in electrons, were calculated using the following equation:

Noise
$$(e) = \frac{6250\left(\frac{e}{fC}\right) * SPICE \text{ noise output } (mV)}{Gain\left(\frac{fC}{mV}\right)}$$

3.1 Adjustment of the Peaking Time

It is very important that the adjustment of the peaking time, the time in the shaper output that it takes for the voltage to reach its maximum, be performed every time one makes an alteration in the SPICE model. The peaking time itself was determined experimentally on the shaper output of the physical setup using a picoprobe, and for practical reasons – the physical setup uses hair-thin wire bonds, and as such it is extremely difficult and time consuming to change the physical model's settings – only the peaking time of the physical setup at 5 steps was used, $1.8 \ \mu$ s. It should be noted that there is nothing special about this particular setting; when the measurement was taken, the physical setup had already been set to 5 steps, and as such it was a matter of convenience.

Adjusting the peaking time of the SPICE model is a relatively simple task. One need only adjust the integrator resistors, R_I1, R_I2, and R_AMP2 until the desired peaking time is acquired. Due to the complex dependence of the peaking time on these resistor values, this is a highly repetitive task, requiring a great deal of guess-and-check work. The only caveat is that all three resistors must remain equal to each other. Given that the only data point that was used was for the 5 step setting, adjustments were made to the SPICE model on that setting and, once the proper values were found, copied to the versions of the models that correspond to the various step settings.

3.2 Parasitic Capacitance

R6	R7 75 35.875	R8	-	R9 35.875	R10	R11	R12	R13	R14 35.875	R15	R16	•		817	R ² 35.8
5	C6	C7	C8	C_parasite1	C9	C10	C11	C12	C13	C14	C15	C16	C_parasite2		C17
5p	.65p	.65p	.65p	1p	.65p	.65p	.65p	.65p	.65p	.65p	.65p	.65p	1p	-	.65p
	, , , , , , , , , , , , , , , , , , ,	✓	⇒	\checkmark	✓	→ ¬	→ ¬					⇒	\Rightarrow	7	7

Figure 7: An excerpt from a detector RC circuit series, with the parasitic capacitors in a red box; each parasite is positioned between every eight RC circuits, corresponding to a single step

It was thought at one point that the noise not being accounted for by the SPICE model could be caused by "parasitic capacitance," a rogue capacitance created by the close channels and wire bonds of the physical system. As can be seen in the above figure, parasitic capacitances were simulated in the SPICE model by placing 1 pF capacitors (chosen by determining what degree of capacitance it would require to make the 13 step model output closely match its measured value) in between each series of RC circuits that represented a "step." The results were relatively good:



Figure 8: A comparison of measured noise values vs. ones generated by SPICE with parasitic capacitors; note that as the number of steps increase, this approximation becomes more accurate

However, there was a problem with this method: when capacitors were introduced to the detector model, they also altered its gain and peaking time. These two things combined made parasite capacitors a less-than-preferable way to incorporate noise in the SPICE model, and when the ideal noise source method mentioned above was observed to perform as well as it did, this parasitic-capacitance approach was discarded.

3.3 The TEMP Command

SPICE's "TEMP" command's function is to adjust the temperature of every circuit element on the whole diagram, thereby increasing the noise. The temperature that was used was 112° Celsius, since this brought the 13 step model into best approximation with the measurements:



Figure 9: A graph comparing the measured noise values to that of the SPICE model when its entirety was raised to a temperature 112°C; note how the noise value at 13 steps matches that of the measurement: this is deliberate, and the basis on which the temperature was chosen

This method has an advantage over the parasitic capacitance method in that using it does not alter gain or peaking time, instead simply increasing the SPICE model's noise output. However, due to the fact that it does increase the temperature of every single element to the same level, a distinctly nonphysical and hard-to-predict effect, it was abandoned in favor of the ideal noise source.

3.4 Ideal Noise Sources

The primary characteristics of an ideal noise source are A) does not in any way alter the gain or peaking time of the voltage/time curve at the shaper output, B) increases SPICE's noise output in a (relatively) predictable way, and C) can increase said noise simply by adjusting the element's temperature. The TEMP method fails requirement B. There were two different ideal noise sources that were used:



Figure 10: Ideal noise source 1, or INS1; sometimes jokingly referred to as a "Taylor Resistor"



Figure 11: Ideal noise source 2, or INS2

The INS1 is a 1 teraOhm resistor, set in parallel at the input to the LSTFE chip model. Its large value and positioning results in zero effect on the gain and peaking time at the shaper output, and thus does not require one to tune the peaking time every time an adjustment is made, unlike the parasitic capacitors. The INS2 is similar to the INS1, except that it is smaller (1 milliOhm) and is placed in the amplifier's feedback loop. This idea was motivated by a discussion in Helmuth and Spieler's *Semiconductor Detector Systems*. In both cases, noise could be increased simply by changing the temperature of the resistor element of the ideal noise source.

We ultimately decided to go with the INS2. This was a physically motivated choice: we were trying to simulate the LSTFE microchip using crude amplifier blocks, and having extra trace resistance in the physical chip is quite believable. The INS1 also only gave an additive noise component, without modifying the noise dependence on input capacitance, an issue that became important while we were performing the procedure outlined in section 3.6.



Figure 12: A comparison of measured values to that of the original SPICE model under the INS2; note that this provides a much better approximation than either of the previous noise-inflating methods. Unlike before, the temperature here was chosen using the lump capacitor tuning method.

The INS2 provided an excellent approximation of the measured noise values. Since the goal of the INS2 was to simulate the voltage-noise contribution of the LSTFE amplifier chip, the temperature of the INS2 could be tuned to reproduce the noise measured when the LSTFE was loaded with a series of single capacitors of various values instead of the distributed RC network associated with an actual sensor. However, while this well-approximated the noise, the gain of the system was very unstable, changing by as much as 36% between the 1-step and 13-step settings.

3.5 Alteration of the Preamplifier Settings

The original SPICE model's preamplifier settings gave it a highly variable gain, going from \sim 2.70 at 1 step to \sim 1.77 at 13 steps, a 36% difference; additionally, the gain of the actual preamplifier was \sim 145, but this is a lesser issue. In order to correct this and, hopefully, gain a better approximation of the noise, it was necessary to adjust the preamplifier settings so that it would stabilize the gain. In order to do this, it was first necessary to determine exactly what the small signal gain at 5 steps was; note that, once again, using the 5 steps setting was entirely a matter of convenience. Fortunately, Sean Crosby's data-taking program provided the gain of the detector setup at a variety of input charges in an easy-to-use graph:



Figure 13: The small signal gain for the 5 step setting: the x-axis is the input charge in fC (2 fC, in this case) and the y-axis is the gain, in V/fC; the gain comes out to about 145 mV/fC

After determining the gain of the 5-step setting, it was necessary to alter the preamplifier until it provided this gain level. After a great deal of guess-and-checking, the following settings were determined to be adequate for our needs:

	Amplifier (E1)	Feedback	Feedback	Gain Stability (%
		Resistor (R_P)	Capacitor (C_P)	drop)
Original	500	10 MΩ	100 fF	36%
Preamp Settings				
Altered Preamp	500,000	584 MΩ	2 fF	<1%
Settings				

Table: Comparison of Original and Altered Preamp Settings

Unfortunately, this did not work as well as hoped, especially not at a small number of steps. In fact, the version of the SPICE model that has the more stable gain also has noise that is in greater disagreement with measured values, especially for small numbers of steps:



Figure 14: A comparison between the two different SPICE models, and the measurement data; note the divergence of the two models at a low number of steps

3.6 The Lump Capacitor Tuning Method

The lump capacitor tuning method was based on measurements taken on the physical model, and revolved around the chip's sensitivity to capacitor load on the detector (which, in the absence of the noise component resulting from the strip resistance, dominates at high loads). It

involves replacing the series of RC circuits that make up the detector model with a single capacitor:



Figure 15: The SPICE setup for the lump capacitor tuning method; measurements were taken at capacitances of 50pF, 100pF, 150pF, and 200pF

The idea behind this was to take four data points – with C_substitute_cap at 50 pF, 100 pF, 150 pF, and 200 pF – at different temperatures of the INS2, until the four data points have a slope of ~9.43. This measured slope was determined experimentally by Sean Crosby:



Figure 16: Noise measured for different values of capacitance using the LTSFE chip and setup described previously; the slope of the best-fit line is ~ 9.43

This particular slope is achieved by adjusting the temperature of the INS2, also part of the model. Once the temperature at which this slope is achieved is determined, it is entered into the INS2's of the main SPICE model at the various step-settings. This is where the temperatures of the previous graphs that used the INS2 came from. As can be seen, the differences are quite dramatic:



Figure 16: A comparison of Crosby's data and SPICE data; as can be seen, without the INS2 the noise slope is virtually flat

4 Results and Analysis

When the appropriate temperature is calculated, and the INS2 is added to both of the SPICE models, the result is:



Figure 17: A comparison between the two SPICE models, while the INS2 is active

As can be seen, neither of these SPICE models are entirely accurate at a small number of steps (small length), although they do converge at large. This would seem to imply that there are additional noise sources in the physical system not accounted for in the model. The fact that the noise curves converge at large ladder lengths, where it is expected that the noise from the detector will dominate, would seem to imply that the unaccounted-for noise source exists in the LSTFE chip – and by extension, does not grow with the length of the detector.

To correct this, it was decided that we would add a small "bump" of noise in quadrature to the noise curves of both models. The value of this bump was determined by extrapolating the noise curves of the SPICE and measured noise curves, without the INS2 active, to 0 steps, and determining the value of the bump by subtracting the y-intercept of each model from the yintercept of the measured. The results are as follows:



Figure 18: A comparison of the SPICE models, with both the INS2 and a "bump" of electrons; the original model was given an additional 270 electrons, and the altered was given 430 electrons

Despite the instability of its gain, the original model is closer to the measured value than the altered model is. However, given the dependence of gain upon ladder length, it is not clear that the original model represented a realistic simulation of the network and its readout, and we take the difference of the two as indicative of the level of systematic error inherent in the SPICE model. Nonetheless, when the result of either model is compared to the measured value, the agreement is good, and suggests that the difference between the naïve (lumped) approximation of Figure 1 and the observed noise values is largely explained by network effects (see Figure 19).



Figure 19: A comparison between the analytic and altered preamp SPICE models

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5 Conclusions

We have used a SPICE simulation of a silicon microstrip detector network, with two alternate models, to explore the difference between observed noise values and those predicted^[1] for a model with lumped network values. Both models show good agreement with the measured noise values at long ladder lengths. While the alternate model exhibits somewhat worse agreement with the measured data than does the original model, its gain varies less with ladder length, matching the behavior observed for the physical setup. We thus take the difference between the two models as a rough reflection of the systematic error in the SPICE simulation.

Further tuning of the model may be achieved by taking other sources of noise into account. While, the current SPICE model may well be an excellent accounting of the noise terms in Eqn. [2] that depend on capacitance, most notably the Johnson noise term $4kTR_s \frac{F_v C^2}{\tau}$, it may not adequately account for other terms, such as I_d , i_{na} , and e_{na} .

The leakage current I_d needs to be measured directly and, due to the lack of features within SPICE in this regard, needs to be added in quadrature to noise measurements on the model. The other two terms are characteristics of the amplifier, the LSTFE chip. While the current model demonstrates that a simple simulation of the chip using a three-stage model is adequate, a more elaborate model would make for a better accounting of the noise, and would be most noticeable at small lengths, where the greatest discrepancy between the SPICE and physical models lies. I would recommend that future studies into this particular SPICE model focus on creating a more accurate model of the LSTFE chip.

Bibliography

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