UNIVERSITY of CALIFORNIA

SANTA CRUZ

**RESISTIVE CHARGE DIVISION
IN MULTI-CHANNEL SILICON STRIP SENSORS**

A thesis submitted in partial satisfaction of the

requirements for the degree of

BACHELOR OF SCIENCE

in

PHYSICS

by

Jerome K. Carman

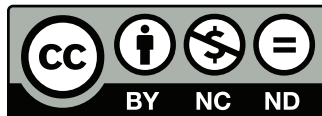20 May 2010

The thesis of Jerome K. Carman is approved by:

_____   _____
Professor Bruce Schumm   Professor David P. Belanger
Technical Advisor   Thesis Advisor

_____
Professor David P. Belanger
Chair, Department of Physics

Abstract

Resistive Charge Division In Multi-Channel Silicon Strip Sensors

by

Jerome K. Carman

Over the past few decades, silicon strip sensors have become the dominant instrument for tracking sub-atomic particles in accelerator beam collisions. These sensors are composed of multiple long thin strips of doped silicon running parallel to each other, and implanted on a bulk silicon crystal of opposite doping. To obtain a particle's position, two coordinates must be measured: one perpendicular to the silicon strips, and the other parallel. For the position coordinate perpendicular to the silicon strips, a significant amount of work has been done in the past to obtain measurement resolutions on the order of micrometers. However, little work has been done to explore methods for obtaining the position coordinate parallel to the strips. Prior experiments have derived this coordinate by adding additional, perpendicularly-oriented layers of sensors, which add material and mechanical complexity to the detector design.

This thesis is motivated by the Silicon Detector (SiD) concept which is part of the International Linear Collider (ILC) project, an international effort working to design a 28km linear e^+e^- particle collider for future high-energy sub-atomic particle experiments. The focus of this thesis is on the implementation of the resistive charge division method to obtain the parallel position coordinate using a single silicon strip sensor, an instrument to which this method has not been applied in high-energy particle detection experiments. To be effective in improving the pattern recognition of particle tracks for ILC physics, a parallel position resolution of $\leq 1cm$ is required with a readout electronics shaping time of less than $3\mu s$. These constraints provide a benchmark with which to gauge the viability of this method for application to the ILC project. To determine this viability, both a printed circuit board and PSpice computer simulation were developed to model a single $10cm$ long silicon strip, with nominal characteristics of $60^{k\Omega}/_{cm}$ and $1.25^{pF}/_{cm}$. These models use

a well-documented method of representing a silicon strip using discrete analog components. In addition, investigation of the effects of signal crosstalk between neighboring strips was performed by extending the PSpice simulation to a five-strip model.

The results of this project show the resistive charge division method to be a viable option for improving the pattern recognition of particle tracks for ILC physics using silicon strip sensors. For a single $10cm$ long strip, it was found that a position resolution of $0.6cm$ can be obtained with an optimum shaping time of $1.8\mu s$. The five-strip model proved to degrade the single strip resolution by 10%-15%, while the optimum shaping time increased to $2.6\mu s$. For both models, position measurements directly correlated with actual signal position, and position resolution proved to be largely independent of signal position. However, due to the high resistance of the silicon strip and the division of the signal between both ends of the strip, signal to noise ratios (SNR) may be undesirably low: the single-strip model resulted in a SNR of 7.6 for a signal originating at the center of the sensor, and the five-strip model resulted in a SNR of 6.6. These low SNR values may impact the precision of the perpendicular coordinate resolution.

Dedication

For Carlos, whose integrity of character, passionate curiosity, and immeasurable kindness will

always be an inspiration.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The International Linear Collider (ILC) is a 500GeV e^+e^- collider proposed to explore fundamental particle physics at an energy effectively comparable to the Large Hadron Collider (LHC). The force behind the conception of this massive 31km collider is the desire to create a cleaner environment for precision measurements which are not possible in noisy $p\bar{p}$ hadron collisions found at the LHC. The relatively relaxed beam repetition rate designed for the ILC is essential to the motivation of this thesis. Roughly three thousand bunches of electrons and positrons collide in $1ms$ pulses at a period of 5Hz (see Figure 1.1). This provides two independent scales of time between possible particle bunch crossings; $199ms$ between beam pulses, and $\sim 300ns$ between bunch crossings within each pulse. The $300ns$ between bunch crossings, combined with the low expected occupancy ($\sim 0.03\, hits/mm^2/bunch\, crossing$ at the vertex detector[3]) of e^+e^- collisions, work in concert to allow relatively large shaping times of $1 - 3\mu s$ without significant risk of information loss.

Figure 1.1: Graphic of the pulsed beam delivery design of the ILC concept.

Motivated by the ILC design project, a tracking study by Chris Meyer et. al.[6] showed a significant reduction in the number of fake particle tracks that originate within the detector volume if a longitudinal segmentation of $\leq 1cm$ for silicon strip sensors is implemented. With the ILC design expectation that 5% of tracks will arise within the detector volume (from secondary decays of

unstable particles), there is a strong argument for a measurement technique that can accomplish a longitudinal position resolution of $\leq 1cm$. One method of implementing this is to physically segment the sensors into $1cm$ lengths. However, the cost of this approach is an increase in the number of readout electronics required compared with the use of longer sensors (since the number of sensors will increase), along with the increased amount of material and power required to service the increased number of sensors.

However, a paper published by V. Radeka in 1974[8] discusses the use of the resistive charge division method for obtaining this position resolution along the longitudinal coordinate of highly resistive electrodes. According to [8], the fractional position resolution obtainable with this method depends only on the electrode capacitance, and *not* the resistance. This is described via the relation

$$\frac{\Delta l}{l} = \gamma \frac{\sqrt{kTC_D}}{Q_t}, \tag{1.1}$$

where $\Delta l = 2.4\sigma$ is the full-width-half-max (FWHM) of the noise Gaussian envelope, k is Boltzmann's constant, T is temperature, C_D is the total capacitance, Q_t is the total signal charge deposited into the sensor, and γ is a unitless coefficient whose value depends on the shaping parameters of the readout electronics.

Unique to this resistive charge division approach, we propose obtaining the large sensor resistance by directly reading out the highly resistive p-type implant of a silicon strip sensor(see Figure 1.2). Typically the p-type implant is coupled to a metalization layer deposited on top of the implant which is then electrically connected to the readout electronics. Common silicon strip sensor designs read out only one side of the sensor; a technique requiring the resistive load on the pre-amplifier (pre-amp) to be small in order to keep series Johnson noise levels low. Hence the motivation for the metalization layer which typically has a resistance on the order of $10^1\Omega$. However, since the resistive charge division method requires the sensor resistance R_D to be significantly larger than the input impedance $|Z_{input}|$ of the readout electronics, the doped silicon implant makes a convenient charge division environment.

The absence of sensor resistance in Eqn. 1.1 is significant since this is what makes resistive charge division appealing. Since this method uses a highly resistive sensor to get the signal charge
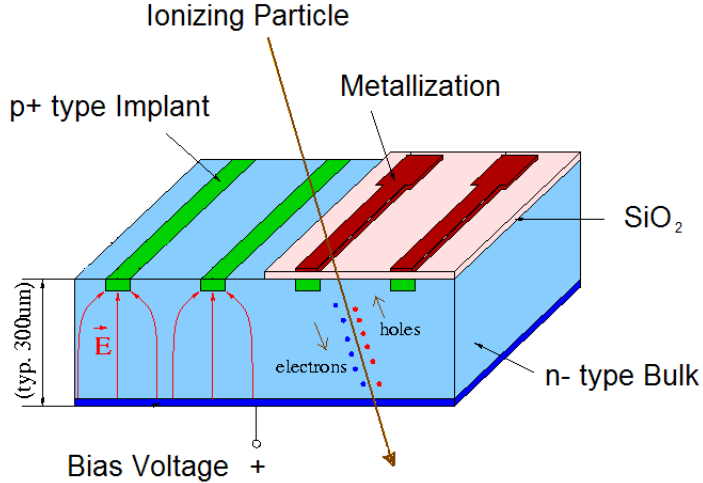
Figure 1.2: Cross section of a silicon strip sensor showing both the p-type silicon implant and the common metalization layer which is not used for the resistive charge division method.

to divide across the length of the sensor, each silicon strip must be read out at both ends. In addition, $R_D \gg |Z_{input}|$ in order for the charge to travel to the input of the readout electronics. Hence, the absence of R_D in Eqn. 1.1 is a key feature relieving the worry that R_D might degrade position resolution via a large contribution from resistive ("Johnson") noise.

A recent conversation with the silicon sensor manufacturer Hamamatsu revealed that a doped silicon resistivity of $60k\Omega/cm$ is achievable. Therefore, this resistivity is used, along with the common sensor capacitance of $1.25pF/cm$, to create a single and five-strip model of a silicon strip sensor using discrete analog components. An actual silicon strip sensor was manufactured specifically for the exploration of the resistive charge division method, but a manufacturing error included a metalization layer rendering them unusable for this project. Therefore, a printed circuit (PC) board model was designed and used to benchmark results from a PSpice computer simulation of the single and five-strip models.

The high sensor resistance necessary for resistive charge division does come at the price of requiring a relatively long shaping time (see Section 2.1.1). The desire for an optimum signal-to-noise ratio (SNR) also increases the shaping time needed to implement this method. This is where the two key features of the ILC design stated earlier come to play. Because the ILC design is capable

3

of accommodating shaping times of $1-3\mu s$, the resistive charge division method is an option worth exploring. In addition, while the concept of resistive charge division has existed in the relevant literature for the last fifty years, there appears to be no literature in the application of resistive charge division as a longitudinal position measurement method for high-energy particle tracking. Along with the unique conditions of the ILC design, the lack of literature on this application has motivated this project.

Chapter 2

Methods

This project is divided into two phases, the first focusing on modeling a single-strip sensor, and the second expanding to a five-strip model to allow the investigation of cross-talk between neighboring strips. The single-strip investigation involves a PSpice simulation as well as a PC board model. The motivation behind these two approaches is to provide a benchmark of the simulation by comparing it's behavior to that of the PC board model. Due to stray capacitances on the final PC board design being too large for a five-strip investigation, this model only uses a PSpice simulation.

2.1 Simulation Design

2.1.1 Sensor Model

As has been done by V. Radeka and others ([1],[2],[4],[5],[7],[8],[9]), a single silicon sensor strip can be approximated by a simple discrete chain of low pass RC filters as shown in Figure 2.1. The resistance of each silicon strip is determined by the material properties of the doped silicon as well as the physical dimensions of each strip. The capacitance of each strip is determined by three factors; the material properties and physical dimensions of the strip, the proximity of the neighboring strips, and the thickness of the n-type bulk that separates the strip from the back plane (see Figure 1.2). This project is based upon the impedance characteristics of a 10cm long silicon strip sensor with $60^{k\Omega}/cm$ and $1.25^{pF}/cm$, resulting in a total single strip resistance and capacitance

5

of $R_D = 600k\Omega$ and $C_D = 12.5pF$ respectively. The resistivity parameter is a value obtained by a recent discussion with Hamamatsu as an achievable characteristic, and the capacitive parameter is a common value for $300\mu m$ thick sensors with $50\mu m$ pitch.
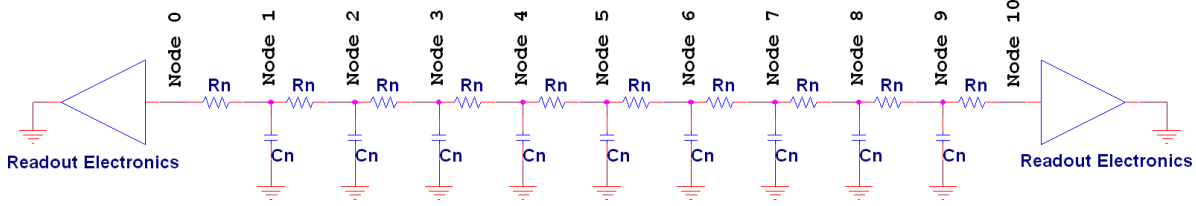
Figure 2.1: Basic schematic of the RC network representation of a single-strip silicon sensor model. The input impedance Z_{input} of the readout electronics is much less than the total sensor resistance R_D.

The high strip resistance due to the doped silicon is used to ensure that $R_D \gg Z_{input}$, where Z_{input} is the input impedance of the readout electronics, thereby causing the readout electronics input to act as a virtual ground. The high resistance comes simply from eliminating the common metal readout strip typically applied atop the length of the p-type silicon implant and instead coupling the readout electronics input directly to the silicon implant (see Figure 1.2).

In order to model a silicon strip sensor with discrete analog components, it must be decided how the total resistance R_D and capacitance C_D of the silicon strip will be divided. The total number of finite resistances must be numerous enough to allow position dependent measurements as well as to sufficiently model a continuously distributed resistance. However, convenience and efficiency offers incentive to minimize the total number of resistors used when designing the printed circuit board model. To determine an acceptable balance between these two conditions, a simple low-pass RC network simulation was constructed using PSpice, with a total resistance of $R_D = 600k\Omega$ and a total capacitance to ground of $C_D = 12.5pF$. In this simulation the number of divisions n was varied resulting in a resistance and capacitance per division of R_D/n and C_D/n respectively. A known charge was injected into various nodes. The voltage signals at both ends of this simple network were compared for the various divisions. For simulations of 10, 30, and 50 nodes, Figure 2.2 shows the result that the number of divisions does not have an appreciable influence on the signal amplitude or propagation time. Therefore, a ten node RC network was chosen to model a

single silicon strip, with each node representing $1cm$. Since the single node RC time constant of the 50-node simulation is $\sim 0.4ns$, which is less than the injection signal rise time used of $1ns$ (see Section 2.2.4), it does not appear necessary to consider a larger number of divisions.
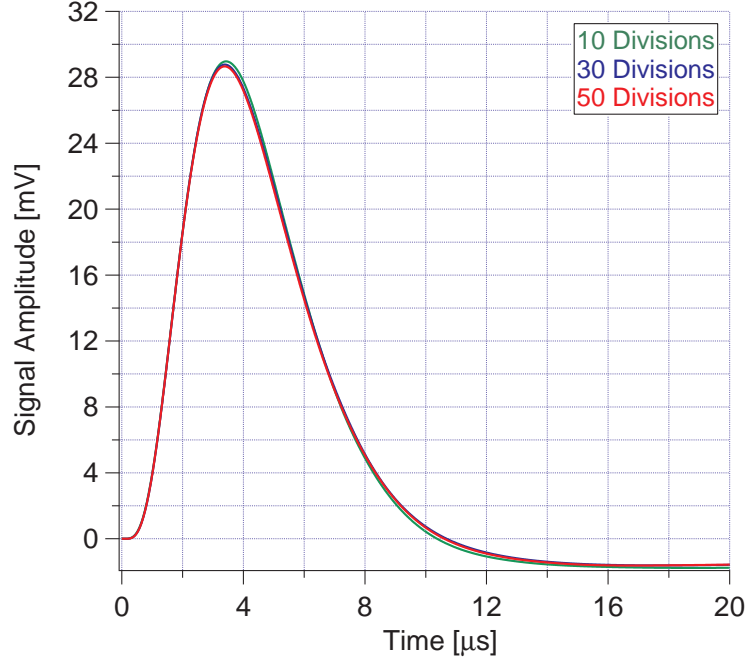
Figure 2.2: Plot of the shaped output of a $3fC$ injected charge across a $600k\Omega$, $12.5pF$ RC network for 10, 30, 50 nodes.

This choice of ten nodes results in the single-strip model values of $R_n = {}^{R_D}/_{10} = 60k\Omega$ and $C_n = {}^{C_D}/_9 = 1.39pF$ (note that there are $n-1$ capacitors in this sensor network model). For the single-strip model shown in Figure 2.1, the capacitive coupling is entirely to ground. For the five-strip model shown in Figure 2.3 C_n must be divided between the capacitance to ground and capacitance to the neighboring strips. Relying on the general experience that 40% of the total sensor capacitance is coupled to ground and 60% is coupled to the two neighboring strips, we chose the values of $C_{n,gnd} = 0.4C_n = 0.56pF$ and $C_{n,nbr} = {}^{0.6}/_2C_n = 0.42pF$ where the factor of $^1/_2$ comes from the fact that $0.6C_n$ is divided between two neighbors. For the outside strips the second $C_{n,nbr}$ is coupled to ground.
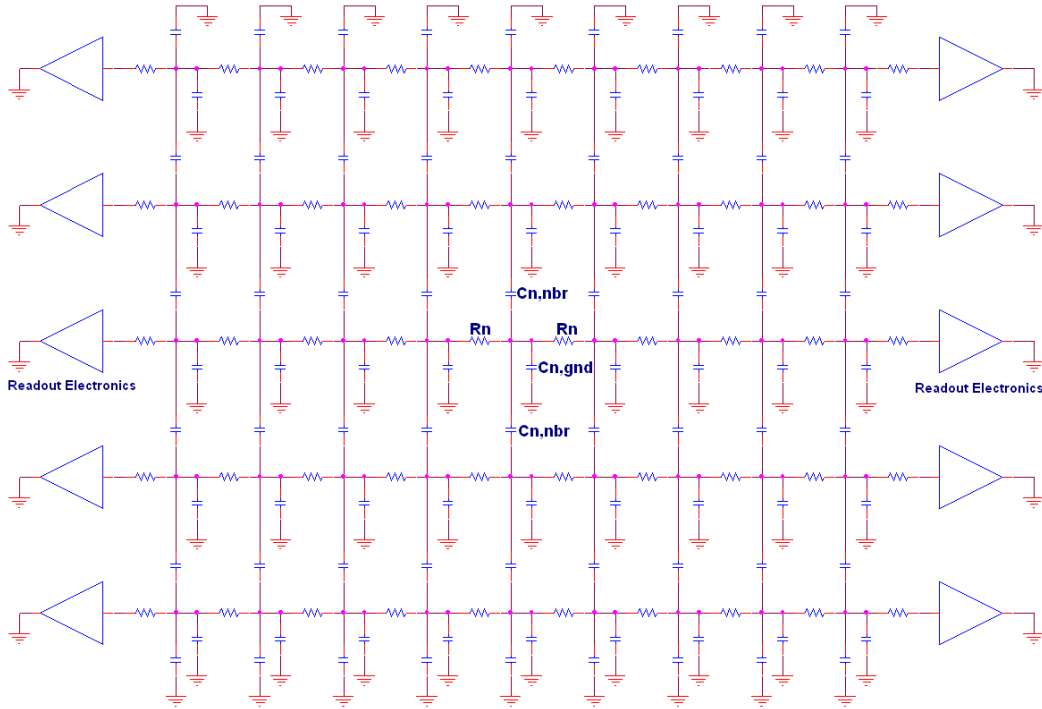
Figure 2.3: Basic schematic of the RC network representation of a five-strip silicon sensor model.

2.1.2 Simulation Of The PC Board Readout Electronics

Considering a single sensor strip, the essential idea is to create a ten node RC network that is terminated on both ends by a charge sensitive pre-amplifier followed by a signal shaper. Design and/or use of application-specific signal acquisition electronics was not the goal of this project. In fact, as is stated below, the readout noise is dominated by the sensor strip resistance rather than the readout electronics. Therefore, emphasis was placed on simplicity by ac coupling the pre-amp through a passive differentiation into a three stage integration shaper.

For the PC board model, the Burr-Brown OPA657 FET-input operational amplifier (op-amp) was chosen for the charge sensitive pre-amp, and the Analog Devices ADA4851 video amplifier was chosen to be used for the two active buffers of the three-stage integration (see Section 2.2.3 for more details about the readout electronics). However, as can be seen in Figure 2.4, only the OPA657 pre-amp was represented by a realistic PSpice model, while the second and third Analog Devices op-amps were modeled via ideal voltage-controlled voltage sources (VCVS). According to simulations, the pre-amp contributes < 1% to the total noise of the system. In addition, of the readout electronics, it is expected that the pre-amp will contribute the majority of the noise

contribution. Based on these two points, it was decided that a more realistic model of the pre-amp alone would be used, and use of an ideal VCVS for the second and third op-amps would provide a sufficient noise result. The benefit of this choice is a simplified simulation model, decreased simulation times, and increased likelihood that a simulation run will converge to a valid result.
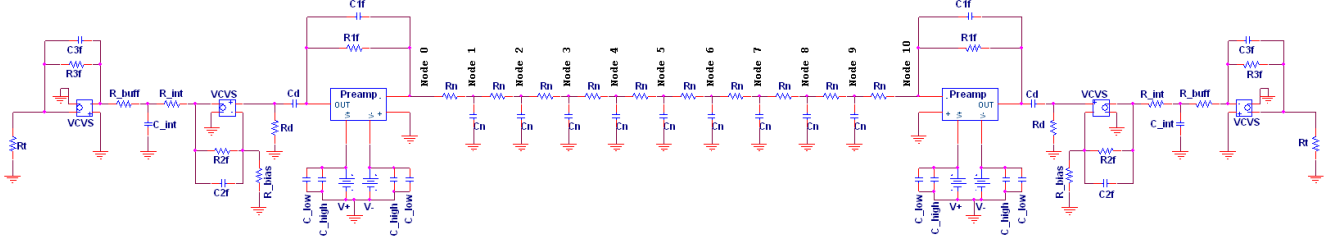
Figure 2.4: Schematic of initial single-strip PSpice simulation design before stray capacitance corrections were added.

2.1.3 Stray Capacitance Corrections

In order to benchmark the simulation with the PC board, stray capacitance corrections were applied (see Section 2.2.2 for measurement details). Both the sensor model, as well as the pre-amp, are sensitive to these stray capacitances. Since the sensor model is effectively a series of low pass RC filters, the stray capacitances affect the rise time of the signal and influence the low frequency bandpass of the sensor. The pre-amp sensitivity exists for two reasons. First, the pre-amp feedback capacitance C_{1f} is small enough such that the stray capacitance of the traces and components form a significant percentage of this capacitance. Second, the pre-amp input is highly sensitive to load capacitances. Therefore, stray capacitance measurements focused on the traces and components that make up the sensor and pre-amp, and the shaper electronics were ignored as they are not sensitive to the relatively small stray capacitance values.

The results shown in Table 2.1 (see Section 2.2.2) were applied to the simulation. This resulted in the final simulation design shown in Figure 2.5. The same corrections are also applied to each strip of the five-strip model. In the simulation model, the stray capacitances $C_{s,R}$ and $C_{s,node}$ were combined into the single stray capacitance value $C_{R,stray} = C_{s,R} + C_{s,node} = 0.09pF$. For both the single- and five-strip models, $C_{s,nbr}$ was ignored.

Figure 2.5: Schematic of the final single-strip PSpice simulation design with stray capacitances added. The integration shaper design is unchanged from that shown in Figure 2.4.

2.2 Printed Circuit Board Design

To provide a cross check of the simulation results, a printed circuit board was designed to emulate a five-strip silicon strip sensor with readout electronics on both ends. The schematic of each of the five identical strips is that shown in Figure 2.4. The design schematic and layout was created using the Mentor Pads® Logic and Layout programs, and the final result was manufactured off-site by Sierra Proto Express using their No-Touch process. The most challenging aspect of this printed circuit board model design was minimization of the stray capacitances to the ground plane since we are dealing with relatively small capacitances (1.25pF / cm). This constraint required a compact design to minimize trace lengths, as well as removal of the ground plane from underneath the sensor strips (see Figure A.3 in Appendix A).

Figure 2.6: Picture of the manufactured printed circuit board model of a five-strip sensor with readout electronics. Only the center strip is loaded with components since the PC board was not used to explore a five-strip model. The wire connected to the center of the board is the charge injection probe.

2.2.1   4-layer board

A four-layer PC board construction was used, the material cross-section of which is shown in Figure A.1 (see Appendix A). The first layer is shown in Figure A.2 and consists of the majority of electrical components and traces. The entire sensor RC network exists on this layer as well as all op-amps and charge injection probe connection points. Each metal trace was made to be of equal length between strips to maintain uniformity, with the exception of the third op-amp output which is not sensitive to small variations in stray capacitance. No traces are long or thin enough to worry about inductive impedances. Note also the presence of a test channel which was used to test different readout designs without risking physical damage to the five main strips.

The second layer is the ground plane shown in Figure A.3 in Appendix A. This metal layer exists over most of the area of the board, with the exception of long rectangular cutouts underneath each sensor strip. These cutouts are intended to reduce the amount of stray capacitive coupling of the sensor components to the ground plane. Strips of ground metal were run between strips to allow ground connections for components as well as to minimize stray capacitive coupling between strips.

The third and fourth layers are respectively $+5V$ and $-5V$ power planes are shown in Figures A.4 and A.5 in Appendix A. The power is distributed via a central connector through large metal traces to three large sections of metal located under each of the left and right sets of readout electronics. Each pre-amp power supply pin filters the power through a 100MHz inductor, and high and low decoupling capacitors are placed in close proximity to ensure peak frequency response. Each set of second stage op-amps share a power filtering inductor and low frequency decoupling capacitor, yet a high frequency decoupling capacitor is assigned to each individual op-amp close to it's power pin. This design applies to the third stage op-amps as well. In addition, since multiple op-amps share the same power plane, a very low frequency $330\mu F$ decoupling capacitor is tied to each power plane. The fourth layer also includes some decoupling capacitor components and traces as well as two large sections of metal that are tied to the ground plane. These were used to tie various sensor strips and nodes to ground via conductive copper tape when performing stray capacitance measurements.

2.2.2 Stray Capacitance Measurements

After the PC board model was manufactured, stray capacitance measurements were made using an Agilent E4980A 2MHz LCR meter. Stray capacitances occur because of materials that carry different voltage potentials, and are determined by the dielectric properties of the materials used as well as the physical dimensions and proximity of components and traces. For the sensor section of the PC board, the total stray capacitance associated with a single node was characterized. The results are shown in Table 2.1. The capacitive coupling between neighboring strip nodes ($C_{s,nbr}$), between adjacent nodes ($C_{s,node}$), and between the node and the ground plane ($C_{s,gnd}$), were measured. In addition, the stray capacitance associated with the resistor components forming the sensor model ($C_{s,R}$) was characterized. For the pre-amp, the stray capacitance to ground of the trace leading to the input ($C_{s,input}$) was determined. The capacitive coupling between the pre-amp feedback component pads ($C_{s,fb}$) were determined as well. Because the stray capacitance to ground $C_{s,gnd}$ was nearly equal to the desired capacitance per node C_n, the stray capacitance was used in place of using physical components. This resulted in a $\sim 9\%$ difference between actual sensor capacitance, and the capacitance used in the single- and five-strip models.

Sensor Nodes	
$C_{s,node}$	$47fF \pm 1fF$
$C_{s,R}$	$43fF \pm 1fF$
$C_{s,nbr}$	$5fF \pm 1fF$
$C_{s,gnd}$	$1.265pF \pm 1fF$

pre-amp Traces	
$C_{s,input}$	$2.186pF \pm 8fF$
$C_{s,fb}$	$60fF \pm 1fF$
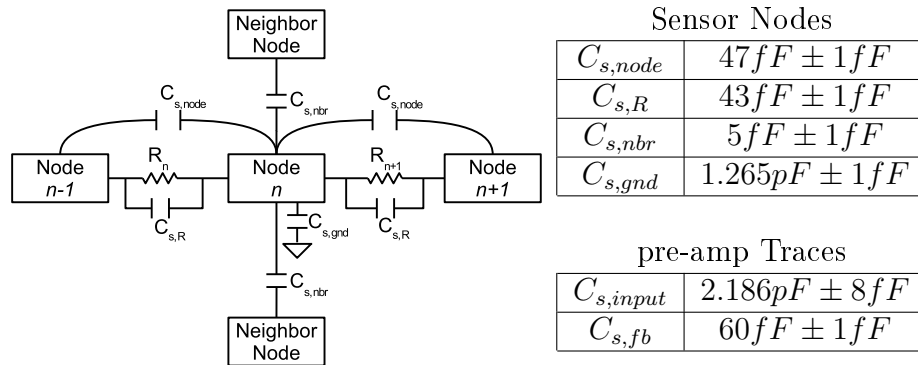
Table 2.1: Stray capacitance measurement results of a single node of the sensor section of the PC board as well as for the pre-amp traces and pads.

The measurement technique used to determine capacitive coupling of traces and pads to the ground plane involved tying the LCR Meter ground to a copper base placed beneath the PC board. This copper base was electrically isolated from the PC board via double-sided tape. This shielded

the PC board, preventing it from coupling capacitively with the surrounding environment. A Kelvin-style probe was used, with one probe tip placed on the object of interest, and the other placed on the ground plane of the PC board (which was not tied to the LCR Meter ground). A $1.0V$ signal was used at $2MHz$, with open and short corrections applied. In all cases, frequency and voltage dependence was negligible, with a $< 2\%$ change in measured capacitance for a frequency of $100kHz$, and a $< 1\%$ change in measured capacitance for a $10mV$ signal.

To determine the stray capacitance between neighboring pads, the LCR Meter ground was tied to the PC board ground plane, effectively canceling out any stray capacitance to ground. In addition, all other pads and traces except the ones under investigation were tied to the PC board ground plane via conductive copper tape. This technique isolated the particular sensor node under investigation from the rest of the PC board to create as clean an environment as possible. A Kelvin-style probe was also used, with a $1.0V$ signal at $2MHz$ and open and short corrections applied. Frequency and voltage dependencies were also negligible for these measurements.

2.2.3   Readout Electronics Design

Motivated by the discussion on signal processing by H. Spieler [10], it was decided that the charge-sensitive pre-amp output signal would be filtered by a three stage integration shaper. There are two important constraints when using multiple integration stages. First, in theory, optimal SNR is achieved by a Gaussian signal response. Spieler shows that, for some number of integration stages j, the shaped output approaches a Gaussian in the limit that $j \to \infty$. Therefore, the more integration stages used, the better the SNR. In order to keep the number of components and size of the PC board reasonable, three integration stages were used ($j = 3$). Second, optimum SNR is achieved when the differentiation time constant τ_d of the charge sensitive pre-amp is equal to the total integration time constant $\tau_i = \sum_j \tau_j$ of the shaper. To accomplish this, the time constant of each of the integration stages were made equal such that $\tau_j = \tau_i/j = \tau_d/j$.

The resulting design is shown in Figure 2.4. Commercial amplifiers were used for the readout electronics since there are plenty of options available on the market that are sufficient for this project. The readout electronics feature a Burr-Brown OPA657 low noise FET input pre-amp

with a 1.6GHz gain bandwidth product (GPB) in a charge sensitive configuration. The inverting design of the charge sensitive pre-amp creates a virtual ground at it's input. This is an important feature needed for the charge division method to work, and is the reason the response time of the chosen pre-amp model is so fast. If a virtual ground is not effectively maintained (i.e the amplifier input impedance Z_{input} is comparable to the sensor impedance Z_{sensor}) then it becomes difficult to perform a position measurement since the signal will begin to "spread out" across the sensor instead of being acquired by the pre-amp.

The differentiation due to AC-coupling the pre-amp with the shaper inherently has a negative voltage swing associated with it. In order to improve the total amount of charge collected, this undershoot is minimized by passing the pre-amp output through a high pass filter with a large time constant. This time constant was chosen such that, in simulation, the total integrated area of the undershoot is less than 5% of the shaped signal. The second and third op-amps are Analog Devices model ADA4851 video amplifiers with bipolar input and 100MHz GPB. The second op-amp is configured to be a non-inverting integrator that provides the first of three integration stages. The output is fed into a passive integration, which then feeds into the third op-amp configured as an inverting integrator. Each integration stage has $\sim {}^1/_3$ of the total integration shaping time τ_i.

2.2.4   Method And Characterization Of Charge Injection

A charge injection probe was built in order to deliver a known quantity of charge to the PC board model (see Figure 2.7). This was designed to simulate a single, perpendicularly incident, minimum ionizing, high-energy sub-atomic particle. It consisted of a capacitor C_{inj} over which a known step function potential V_s was applied. A LeCroy 9210 Pulse Generator was used to create this step function potential with a $10mV$ amplitude (1.0V over a 40dB attenuator), $1ns$ rise and fall time, $40ms$ width, and $400ms$ period. The charge injection capacitor C_{inj} was soldered in series between a 50Ω coaxial cable and a two pin connector that allowed it to be connected securely to any node of the PC board. The second pin of this connector joined the PC board ground to the ground shield of the coaxial cable. A 50Ω termination resistor R_{term} was used at the connector end in order to match the impedance of the cable and prevent signal reflections.
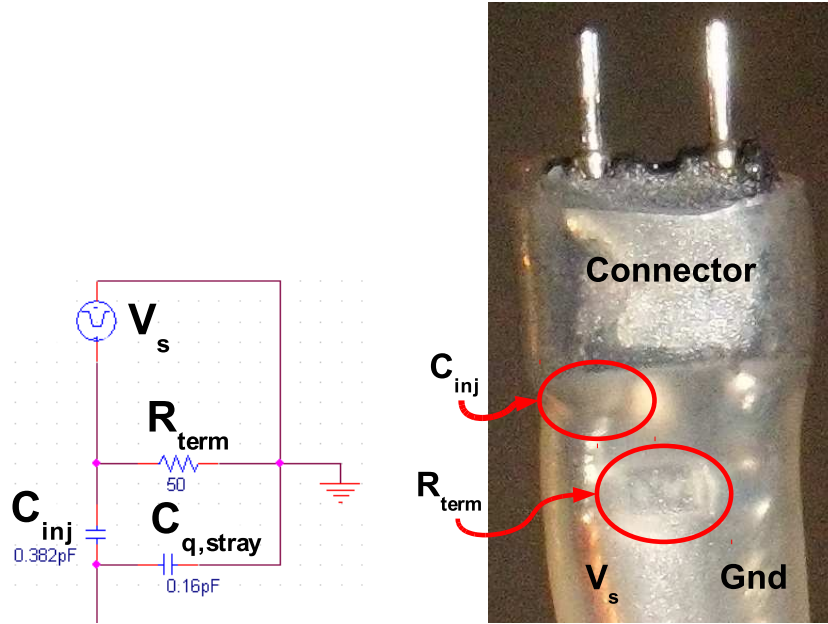
Figure 2.7: Picture and schematic of the charge injection probe used to deliver a known charge signal to the PC board as well as both single and five-strip simulation models. The schematic shows explicitly the stray capacitance due to the connector.

To make the probe sturdy enough to handle without risking the integrity of the capacitor's solder connection, the whole probe tip was encased in epoxy, and shrink tubing was applied for added strength. However, there is a risk that the added epoxy has chemical properties that can alter the effective capacitance of C_{inj}. Therefore, after construction, C_{inj} was measured using the Agilent E4980A 2MHz LCR Meter and a kelvin-style probe with the coaxial shield tied to the LCR Meter ground. This measurement resulted in $C_{inj} = 0.382pF \pm 0.010pF$. For a pulse step of $10mV$, the total injected charge would be $Q_{inj} = 3.82fC \pm 0.10fC$.

However, it was decided that characterization of the capacitive coupling between the two pins of the connector was prudent in order to determine if it is significant compared with the sensor node capacitance C_n. Measuring the connector alone without the cable or capacitor connected, a stray capacitance of $C_{q,stray} = 0.1551pF \pm 0.1fF$ was found which is roughly 11% of C_n. This is a large enough percentage to cause some concern. Therefore a PSpice simulation was done for which the charge injection probe, modeled as the schematic shown in Figure 2.7, was connected to nodes 1 and 5 of the single-strip sensor model shown in Figure 2.5. A $10mV$ potential with the same characteristics as specified above was applied. The current was then measured and integrated at

the output of C_{inj} and at the input of $C_{q,stray}$ to determine the amount of charge that leaks through $C_{q,stray}$. It was found that 2.5% of Q_{inj} is pulled away by $C_{q,stray}$ for a node 5 injection, and 2.4% of Q_{inj} is pulled away by $C_{q,stray}$ for a node 1 injection. Applying the 2.5% result, this translates into an effective charge of $Q_{eff} = 3.72fC \pm 0.10fC$ injected into the sensor model. This value of Q_{eff} is used as the actual amount of charge injected for all results in this paper.

2.3 Optimum Readout Shaping Times

The resistive charge division method requires a linear signal response with respect to position in order to be effective; a feature that improves with longer shaping times. Non-linearity in signal response with respect to position is due to a ballistic deficit[10]. For shaping times less than the signal propagation time, the pre-amp responds too quickly, and the signal begins to recede towards the baseline before the entire amount of charge has reached the pre-amp input. This linearity constraint is the reason for the relatively long shaping times used for this method. On the other hand, the parallel noise contribution from the sensor resistance is directly proportional to the shaping time[8]. The affect of this is a drop in SNR for long shaping times. Thus, an optimum shaping time exists that maximizes SNR and minimizes ballistic deficit.

Because the optimum shaping time depends on the impedance characteristics of the sensor network (which affect the propagation time of a signal across the network), it is convenient to use a method for determining the optimum shaping time that is based on the signal propagation time T of the sensor network. The optimum shaping time can then be expressed as a multiple αT of this propagation time. For the single-strip model, the signal propagation time was determined via simulation by taking the sensor network shown in Figure 2.5, removing the readout electronics and replacing them with a $6k\Omega$ resistor (which approximates the input impedance of the pre-amp), injecting a charge into node 1 of the sensor network, and measuring the resulting voltage signal at node 10. The rise time is measured from $t = 0$, when the signal is injected into node 1, to the peak signal amplitude, and is the longest possible rise time that the pre-amp could encounter given this sensor model. The single-strip model propagation time result was $T_{single} = 0.80\mu s$. The same process was used for the five-strip model, with stray capacitances included and $6k\Omega$ termination

16

resistors, resulting in $T_{five} = 0.57 \mu s$.

To determine the optimum shaping time, different values of the multiplier α were explored, and the SNR and linearity of each setup was evaluated with the PSpice simulation. For the exploration of the single-strip model, all resistors of the readout electronics were fixed to the values shown in Table B.1 in Appendix B in order to keep the DC gain of all three op-amps fixed, thereby removing this as a variable. The value of the pre-amp feedback resistor R_{1f} (refer to Figure 2.5 for readout electronics component labels) was chosen to be as large as possible while maintaining the stability of the pre-amp, and all other resistor values were chosen to keep the DC gain of the two Analog Devices op-amps low in order to maintain a wide bandwidth response. The exception to this was for the $^1/_4 T_{single}$ shaping, for which $R_{1f} = 2.8 M\Omega$ was used because the pre-amp could not drive the small feedback capacitance needed to use the larger $5.65 M\Omega$ value.

To set the capacitor values, the readout electronics model was used in isolation without the sensor model connected to the pre-amp input. A charge signal was applied directly to the pre-amp input, with the $1ns$ rise time of the signal creating an approximate delta function. Looking at the output of the pre-amp, the feedback capacitor was varied such that $C_{1f} = {^{\tau_d}/_{R_{1f}}} = {^{\alpha T}/_{R_{1f}}}$. Once C_{1f} was set, the first integration stage feedback capacitor C_{2f} was varied such that the rise time at the output of the first integration stage was $^{\tau_i}/_3 = {^{\alpha T}/_3}$. Because the signal on the input of the first integration stage is already shaped by the sensor and pre-amp, $C_{2f} \neq {^{\alpha T}/_{3R_{2f}}}$ as basic RC time constant theory dictates. Therefore C_{2f} was set via trial and error by varying the capacitance until the rise time was within $\pm 5\%$ of $^{\alpha T}/_3$. This same process was used to set the second integration stage capacitor C_{int} such that the rise time at the output of R_{int} was within $\pm 5\%$ of $^2/_3 \tau_i = {^2/_3} \alpha T$. The third integration stage feedback capacitor C_{3f} was set such that the rise time at the output of the third op-amp was within $\pm 5\%$ of $\tau_i = \alpha T$. The resulting component values are summarized in Table B.1. Because the five-strip model involves a more complex RC network resulting in a longer signal propagation time, this same process was repeated to determine the optimum shaping time for this model. The components used for this investigation are shown in Table B.2 in Appendix B.

2.4   Signal Acquisition And Analysis

PC board studies were conducted for the single-strip model only; therefore only the center strip of the PC board was used. The output of the third integration stage on both ends was connected to a female BNC connector. For shaped output signal analysis, the left and right output connectors were ac coupled via a large $22\mu F$ capacitor to their own 50Ω terminated Tektronix 640A oscilloscope input channel. A $Q_{eff} = 3.72fC \pm 0.10fC$ charge signal was injected at various node points along the length of the sensor model using the charge injection probe described in Section 2.2.4. The resulting oscilloscope waveforms were averaged over 100 waveforms on the oscilloscope, then downloaded onto a computer via GPIB through a National Instruments GPIB-to-USB adapter. Custom C++ programs were used with ROOT (an open source C++-based data analysis framework) to store, analyze, and plot the downloaded waveforms. In some cases, MatLab and IGOR were used for plotting, yet all numerical analysis was performed using C++ scripts. A comparison of the shaped output waveforms between the simulation and PC board can be found in Figure 3.3 in Section 3.2.

2.5   Noise Analysis

2.5.1   Simulation

Noise analysis of the PSpice simulation used the V(ONOISE) Spice function. A frequency analysis was run using the optimum shaping setup as specified in Section 2.3 with the V(ONOISE) function evaluated at the output node of the third integration stage op-amp. A sinusoidal current source, with a one ampere amplitude used to avoid unit conversion, was connected to the sensor model (the location is arbitrary) as the frequency source needed by the Spice function. The simulation was run in the frequency domain over the range of 30Hz - 300MHz so as to compare with PC board noise measurements (see Section 2.5.2). To find the total noise of the simulation model the calculated V(ONOISE) result, which is in units of $\mu V/\sqrt{Hz}$, is used in the following spice command[11]

$$\sigma_{sim} = sqrt(S(V(ONOISE) * V(ONOISE))), \tag{2.1}$$

where "S" is the Spice command that performs integration over the specified 30Hz - 300MHz range. The total noise result is taken from the point where σ_{sim} has leveled off with respect to frequency, indicating that there is no additional noise contribution from higher frequencies (see Figure 3.7).

2.5.2 PC Board

An initial trace merging method[10] was used to get a rough idea (within $\pm 25\%$) of the expected noise from the PC board model. This was used as a sounding board to catch any egregious errors in the two additional noise measurement methods used which are described below. The trace merging method involves using an analog oscilloscope. The output of one side of the PC board model, which is powered and has no injected charge signal, is connected to a 50Ω splitter, the two outputs of which are connected to two analog oscilloscope input channels. The input channels are 50Ω terminated and DC coupled. The oscilloscope is triggered off an arbitrary external signal. The noise signals on the two oscilloscope channels (which, recall, are each $^1/_2$ the amplitude of the single noise signal due to the splitter) are then carefully merged visually until one larger signal replaces the two separate signals. This resulting larger signal roughly represents a Gaussian envelope of the noise. The two oscilloscope channels are then grounded, and the voltage difference between the two offset channels is measured. This voltage difference corresponds to the full-width-half-max parameter of the Gaussian envelope allowing the relationship $\Delta V \simeq 2.4\sigma$ to be used to approximate the noise of the PC board model. Since a splitter was used the measured amplitude is $^1/_2$ the actual amplitude. Therefore

$$\sigma_{trace} = \frac{2}{2.4}\Delta V. \tag{2.2}$$

A more rigorous PC board noise measurement used an HP 4195A spectrum analyzer. As shown in Figure 2.8, the entire board was placed inside an aluminum box that acted as a Faraday cage to minimize outside electromagnetic interference. The spectrum analyzer has a 1Hz - 500MHz bandwidth capability. For all noise measurements a frequency range of 30Hz - 300MHz was used. This was done to avoid the functional limits of the instrument yet still include frequencies well
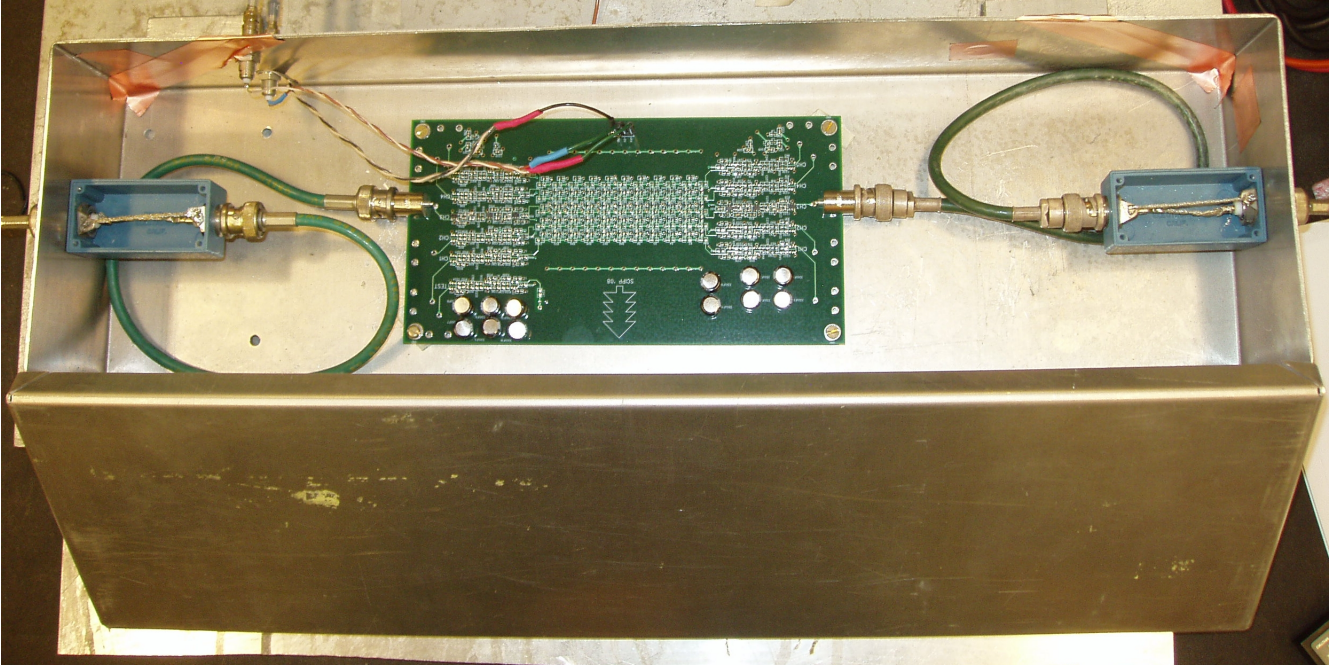
Figure 2.8: Picture of the PC board model inside an aluminum Faraday cage used for signal and noise analysis.

below and above the bandwidth of the readout electronics. The specific instrument settings used are detailed in Table 2.2. The combination of the IRNG3 and ATT2=40dB settings result in a 0dB signal attenuation. Using the auto-bandwidth option, which scales the bandpass of the instrument depending on the frequency being sampled, the spectrum analyzer sweeps the specified frequency range and provides a plot of the noise density spectrum in units of $\mu V/\sqrt{Hz}$ in a logarithmic frequency domain. This plot was also downloaded onto a computer via GPIB through a National Instruments GPIB-to-USB adapter and analyzed using custom C++ and ROOT code. An average spectrum was obtained by acquiring twenty independent spectrum sweeps which were then combined such that each data point in the final noise density spectrum was determined by the relation

$$n_i = \frac{1}{\sqrt{20}} \sum_{j=1}^{20} \left(\frac{\mu V}{\sqrt{Hz}} \right)_j. \tag{2.3}$$

In addition, an averaged background noise density spectrum was obtained using the same method, except without the PC board connected. This averaged background spectrum was subtracted from each corresponding data point of the averaged noise density spectrum in an effort to remove any noise contribution from external electromagnetic interference as well as from the spectrum analyzer

itself.

Spectrum Analyzer Settings	
FNC2	Set to spectrum configuration
PORT2	Select T1 input
SAP6	Select $\mu V/\sqrt{Hz}$ units
NOISE1	Turn on noise marker
VFTR0	Turn off video filtering
CPL1	Set to auto-bandwidth
IRNG3	Set input range to high sensitivity
ATT2=40dB	Sets input attenuation for T1

Table 2.2: Detail of the spectrum analyzer settings used.

The total noise is then determined by numerically integrating the final noise density spectrum. This is again done with C++ code using the following function

$$\sqrt{\sum_{i=1}^{N} \left[(n_i)^2 \cdot \Delta f_i \right]} \tag{2.4}$$

which results in a single number representing the total noise of the single-strip sensor model. Note that $\Delta f_i = f_{i+1} - f_i$ for each data point n_i.[1] For these measurements, the highest possible data set resolution of 401 data points per density spectrum was used. Also, since a logarithmic scale was used, Δf_i increases for each data point. A plot of the single-strip noise spectrum can be found in Figure 3.5 in Section 3.3.

A final noise measurement was performed using the Tektronix 640A digital oscilloscope. A charge signal was injected into node 5 of the PC board and the shaped signal (not averaged) of one side of the center strip was acquired on the oscilloscope. Two thousand waveforms were downloaded onto a computer via GPIB over a roughly 10 minute period such that a statistically significant distribution of the peak signal amplitude could be obtained. The point in time corresponding to the average peak signal amplitude was determined (i.e. the rise time). C++ and ROOT code was used to acquire and histogram this data point (associated with the determined rise time, regardless of whether or not this exactly corresponded to the peak amplitude of the particular waveform) from the 2000 waveforms. The MINUIT function fitting package (included in the ROOT framework) was

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[1]Δf_i is not related to the different bandpass frequencies used by the auto-bandwidth feature of the spectrum analyzer.

used to fit a Gaussian envelope to this histogram. The calculated 1σ width of this fitted Gaussian was then used as the total noise value $\sigma_{spectrum}$. Results are shown in Table 3.1 in Section 3.3.

Chapter 3

Results

There were three main steps to determining the position resolution of this sensor design. First the optimum shaping time was determined, second the shaping characteristics and RMS noise results of the simulation were benchmarked with the PC board, and third the correlation between the left- and right-side signals was quantified. Results are presented in this order, with the five-strip model results included within each section. An additional section showing the investigation of SNR dependence on sensor resistance and capacitance concludes these results.

3.1   Optimum Shaping Time

The method of finding the optimal shaping time as described in Section 2.3 was repeated for various values of the multiplier α, the results of which are compared in Figure 3.1. The left plot of the relative SNR is made by normalizing each result to a maximum SNR of 1.0 for each curve, and clearly shows the ballistic deficit effect resulting in a non-linear response for short shaping times. The right plot of the absolute SNR shows the degradation of SNR for very long shaping times. These measurements show the $2.5T_{single}$ shaping time, shown as the blue curve in both plots, to have the best SNR for nodes far from the pre-amp input. In addition, while there is some noticeable non-linearity in SNR with this shaping time, it does not appear to be worth the reduced SNR to obtain a more linear response, especially in light of the position measurement and resolution results obtained with this shaping time (see Section 3.4).

Therefore, the optimum single-strip model shaping time is $2.5T_{single} = 2.0\mu s$, with $T_{single} = 0.80\mu s$. Using the same method, the optimum shaping time for the five-strip model was found to be $4T_{five} = 2.27\mu s$, with $T_{five} = 0.57\mu s$. The shaping component values used to obtain Figure 3.1 are shown in Tables B.1 and B.2 (see Appendix B) for the single and five-strip models respectively. As shown in Figure 3.2, a $5\% - 6\%$ decrease in SNR is found for the five-strip model. Comparing with the prediction by Radeka (1974) of an optimum shaping time of $\sim 3.9T_{single} = 3.1\mu s$ for this single-strip sensor model, our results appear to be an improvement both in shaping time and SNR. The reason for this is likely the constraint by Radeka that the non-linearity must be $< 0.2\%$. This may also be the reason we observed a slightly better longitudinal resolution than the prediction, as is discussed in Section 3.4.
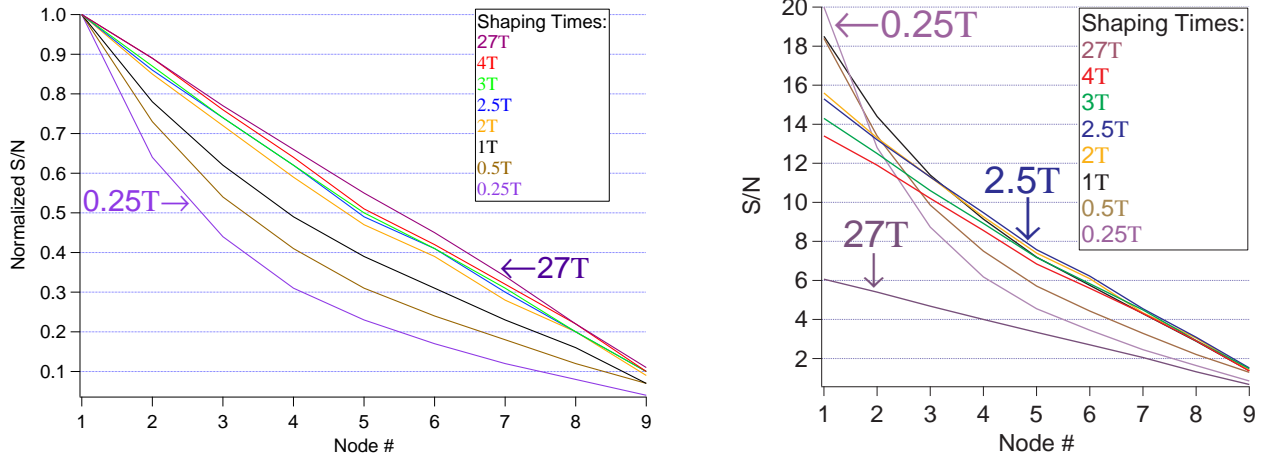

Figure 3.1: SNR and linearity comparison of various shaping times for the single-strip model with stray sensor and pre-amp capacitances. The left plot of the relative SNR shows the presence of ballistic deficit for short shaping times. The right plot of the absolute SNR shows the degradation of SNR due to increased parallel noise contribution for long shaping times.
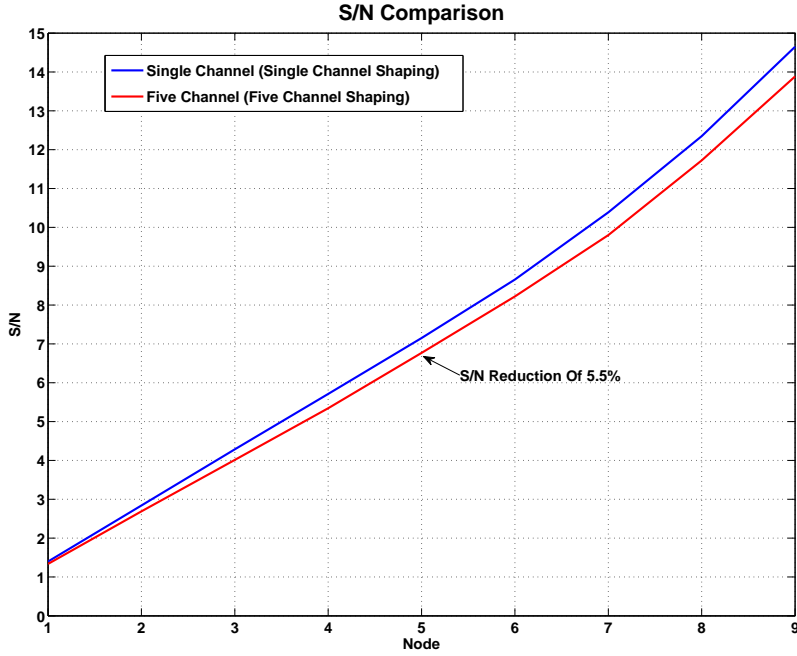
Figure 3.2: SNR comparison between the single and five-strip models.

3.2   Shaped Signal Results

A comparison of the shaped output signal between the single-strip simulation and PC board models can be found in Figure 3.3. Results show good agreement between the simulation and PC board, with rise times differing by $\sim 5\%$ and e^{-1} decay times by $\sim 2.5\%$. Since it is expected that the simulation will have a different, likely larger, gain than the PC board model, the gains of the two models were measured roughly to be $18.7^{mV}/_{fC}$ and $15.9^{mV}/_{fC}$ for the simulation and PC board respectively. These gain measurements were used to scale the simulation output signal. As can be seen by the discrepancy in peak amplitude, we appeared to be off by roughly 5% in our gain measurements. This is not a concern, however, since SNR, and hence position resolution, results are not dependent on readout gain, so the discrepancy was not pursued. In addition, the shaped output, converted to charge at the input of the preamp, of the five-strip simulation model is shown in Figure 3.4 in comparison with the single-strip output signal. A $\sim 2.5\%$ increase in peak amplitude is measured in with the five channel model at the center node.
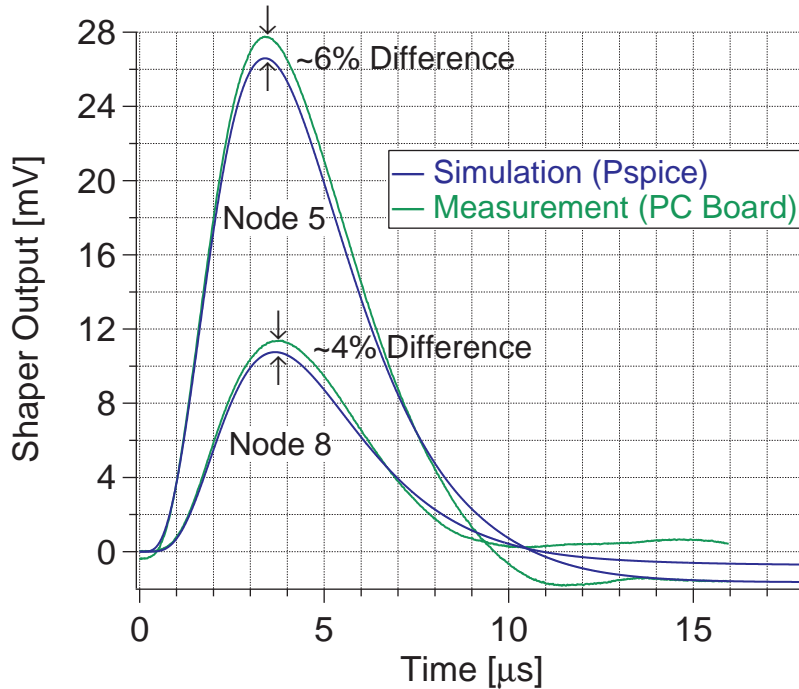
Figure 3.3: Comparison of the shaped output signal for the simulation and PC board single-strip models. Shown are results for node 5 and node 8 charge injections.

3.3 Noise Results

Resulting single-strip noise results can be found in Table 3.1. The noise was converted to $[fC]$ by using the relevant gain as discussed in Section 3.2. The averaged noise density spectrum from which the spectrum analyzer result is derived is shown in Figure 3.5. A Gaussian envelope fitted to the histogram of peak signal amplitude points acquired from the digital oscilloscope is shown in Figure 3.6. The simulation mV noise result was scaled by the simulation and PC board gains for comparison, the result of which shows good agreement. The average noise result of $\sigma_{single} = 0.24fC$ is used for the single-strip model. This result, together with the shaped signal comparison of the previous section, shows that the PC board model provides a successful benchmark of the simulation.
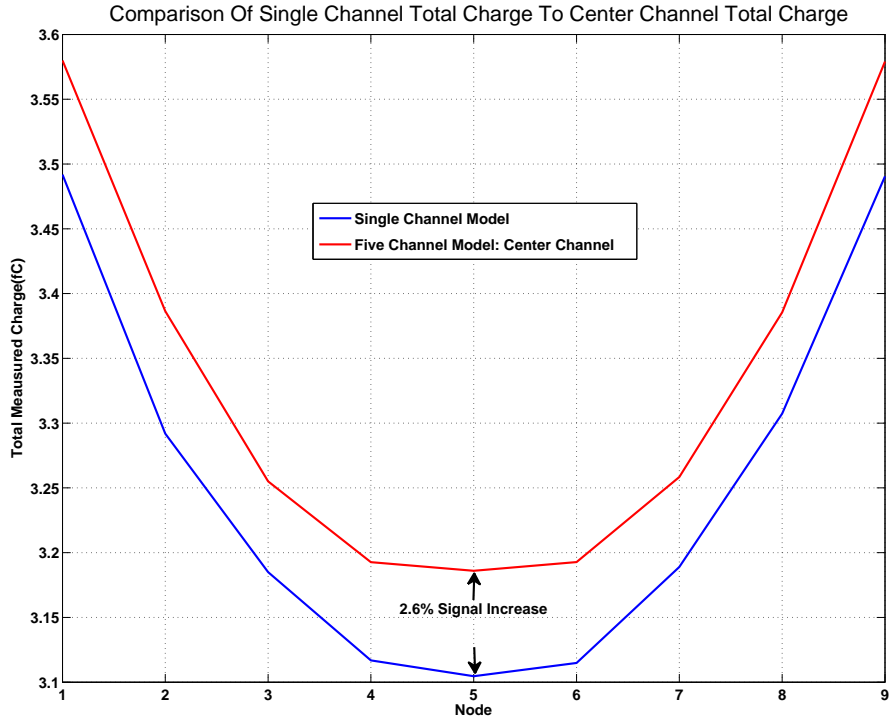
Figure 3.4: Comparison of the center strip shaped output signal of the five-strip simulation model with the single-strip model. Shown is the total charge collected from both ends of the channel.

Single-Strip Model Noise Results		
Measurement	Noise $[mV]$	Noise $[fC]$
Trace Merging	3.67	0.23
Spectrum Analyzer	3.80	0.24
Fitter Gaussian RMS	4.01	0.25
PSpice Simulation	3.79	0.23

Table 3.1: Total noise results for simulation and PC board models. The simulation result was scaled by the ratio of the gains for comparison with PC board results.

In addition, the five-strip model noise simulation shown in Figure 3.7 indicates a $\sim 8\%$ change in total noise compared with the single-strip model.

3.4   Position Measurement And Resolution

To determine the fractional position of an injected signal using the PC board, the relation

$$P = \frac{x}{1+x},\tag{3.1}$$

27

Averaged Noise Spectrum
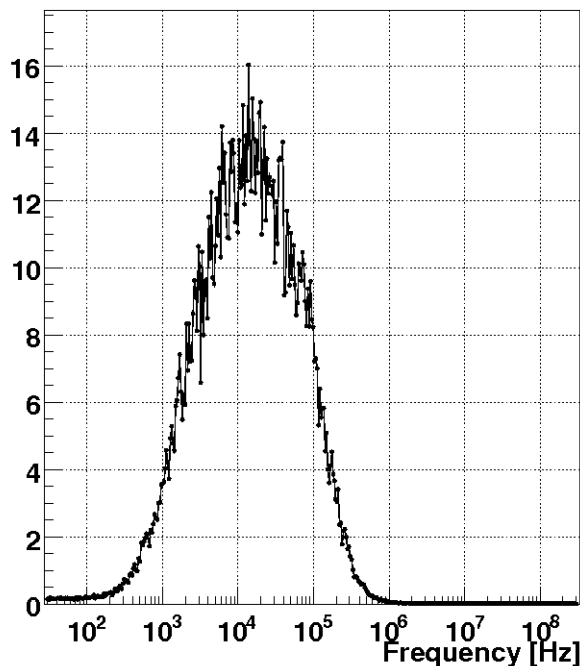

Figure 3.5: Plot of the averaged noise density spectrum for the single-strip PC board model. The vertical axis is in units of $\mu V/\sqrt{Hz}$, the values of which were determine using Eqn. 2.3. An average background density spectrum has been subtracted.

is used, with

$$x = \frac{Q_r}{Q_l}, \tag{3.2}$$

where Q_r is the charge measured by the right side of the sensor, and Q_l is the charge measured by the left side. Taking the peak signal voltage from the left and right sides and converting to charge with the PC board gain of $15.9 mV/fC$ resulted in the position measurements shown in Table 3.2. The top plot of Figure 3.8 of the measured position with respect to actual position shows the resistive charge division method to be effective for position measurement. These measurements are compared to (*not fitted by*) a simple y=x function, shown by the dashed line, to emphasize the linearity of the charge division within the resistive network.

The position resolution is calculated using the relation

$$\sigma_P = \left| \frac{dP}{dx} \right| \sigma_x = \left(\frac{1}{(1+x)^2} \right) \sigma_x, \tag{3.3}$$
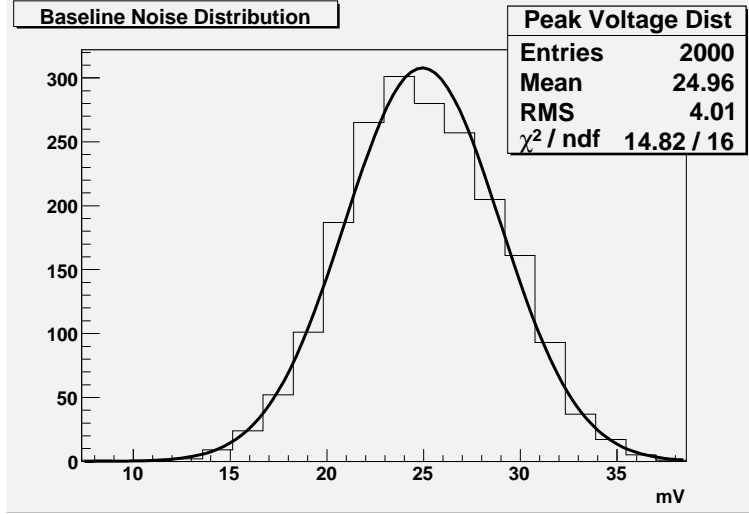
28

Figure 3.6: Plot of the Gaussian envelope fitted to the histogram of 2000 peak amplitude data points. This is a taken from the single-strip PC board model with a charge signal injection at node 5.

with

$$\sigma_x = x\sqrt{\left(\frac{\sigma_r}{Q_r}\right)^2 + \left(\frac{\sigma_l}{Q_l}\right)^2 - 2\rho\left(\frac{\sigma_r}{Q_r}\right)\left(\frac{\sigma_l}{Q_l}\right)}, \tag{3.4}$$

where ρ accounts for the degree of correlation between the left- and right-side signals. Radeka predicted a negative correlation between the left and right signals for shaping times $> {}^1\!/_2 R_D C_D$[8]. This negative correlation is due to reading out both ends of the sensor, and effectively worsens the position resolution. This can be explained intuitively by considering that a positive signal fluctuation on the left end of the sensor will pull charge partially from the sensor network, and partially from the pre-amp on the right end causing a corresponding negative signal fluctuation on it's input. Both the positive left side signal fluctuation and negative right side signal fluctuation work together to shift the measured position towards the left side. Figure 3.9 shows a correlation plot of the left and right side signals. Using Eqn. 3.5, a correlation coefficient of $\rho = -0.61$ was found with the equation

$$\rho = \frac{<r_i l_i> - <r_i><l_i>}{\sqrt{\left(<r_i^2> - <r_i>^2\right)\left(<l_i^2> - <l_i>^2\right)}}, \tag{3.5}$$

where r_i is the right side peak signal amplitude, and l_i is the left side peak signal amplitude.
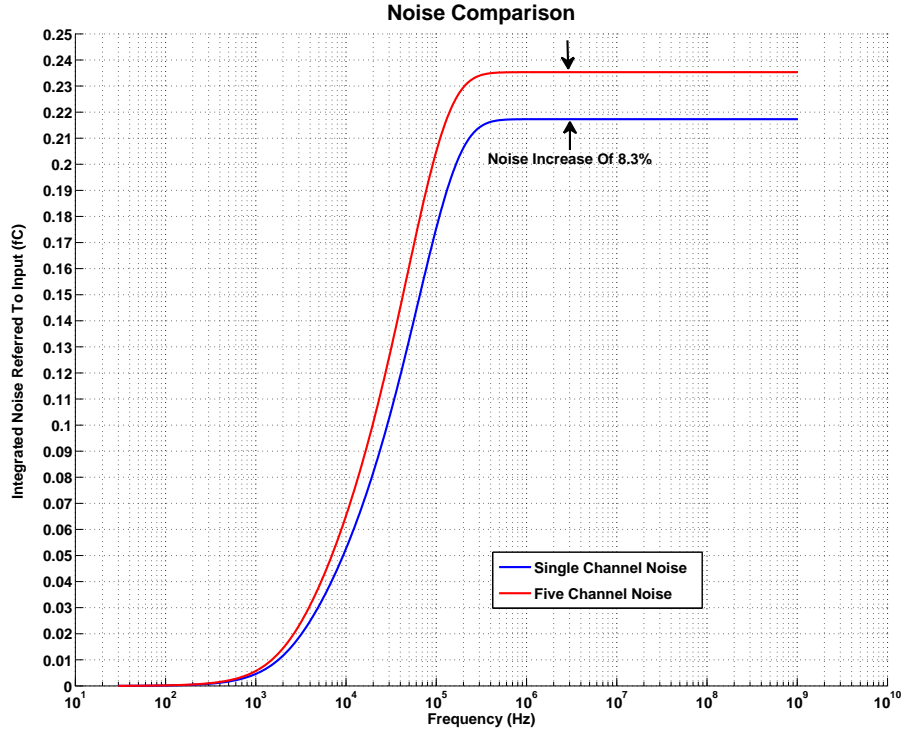
Figure 3.7: Comparison of single and five-strip model PSpice simulation integrated noise curves.

Using the data shown in Table 3.2, with Eqns. 3.3 and 3.4, the fractional position resolution was found to be $\sigma_P = 6.1\%$ of sensor length by averaging the resolution results of each node.[1] For the $10cm$ long silicon strip sensor modeled here, this translates into a resolution of $6.1mm$. The position resolution results are plotted in the lower plot of Figure 3.8, which shows the position resolution to be largely independent of position. This result meets the resolution goal specified by Meyer et. al.[6].

We compared this result with the prediction (Eqn. 1.1) of the 1974 Radeka paper [8]. For $k = 1.38 \times 10^{-23} \left[m^2 kg / s^2 K \right]$, $T = 300°C$ for room temperature, $C_D = 12.7pF$, $Q_T = 3.72fC$, and $\gamma = 2.54$ as used by Radeka, Eqn. 1.1 estimates the fractional resolution to be $\frac{\Delta l}{l} = 0.157$. Δl represents the full-width-half-max value of the Gaussian envelope. Therefore, using the fact that

$$\Delta l = 2.4\sigma, \tag{3.6}$$

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[1]It must be noted that the number of significant figures reported in Table 3.2 for σ_r, σ_l, and σ_P do not follow convention. This was done intentionally so as to show that σ_P measurements did vary slightly with respect to position so as to avoid suspicion of these results. In addition, it is felt that $\sigma_r = \sigma_l = 0.24fC$ is a more honest presentation of the readout noise rather than the $0.2fC$ that convention would require given the $\sim 20\%$ difference between the two numbers.
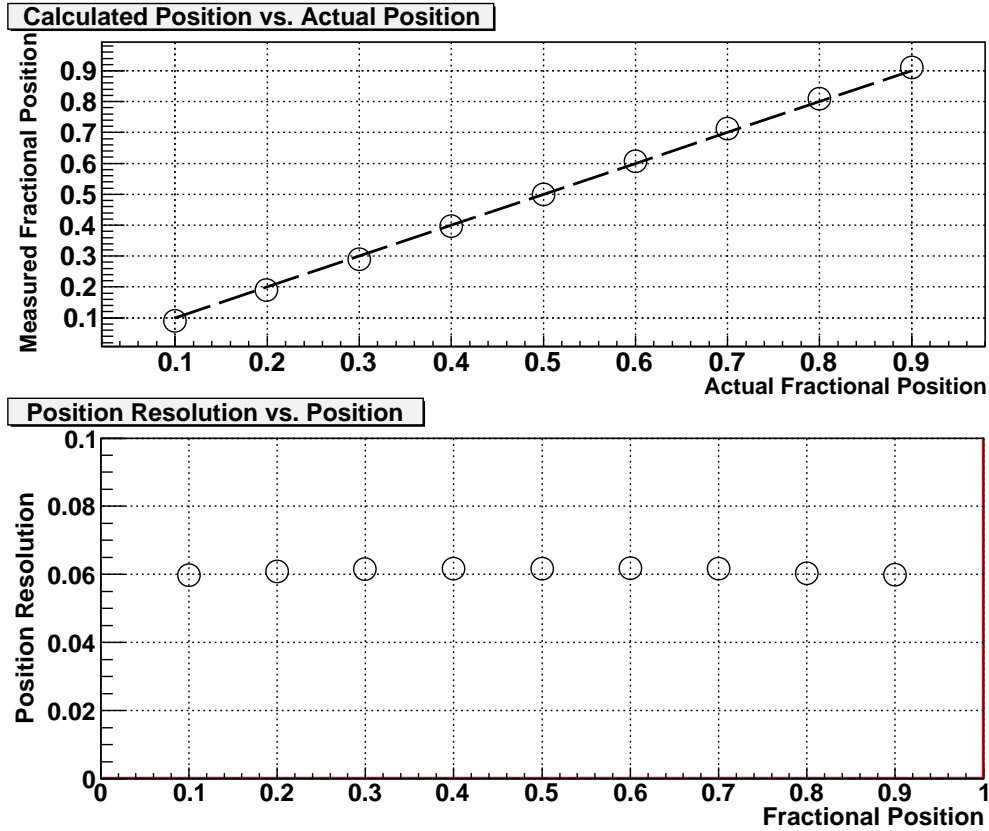
Figure 3.8: The top plot is the measured longitudinal position compared with the actual signal position. The bottom plot shows the position resolution with respect to node number (fractional position).

theory predicts a fractional position resolution of $\sigma_{theory} = 6.5\%$ of sensor length, in good agreement with, but slightly greater than, σ_P. Recall, however, that the requirement by [8] that the non-linearity be $< 0.2\%$ is at the expense of SNR (see Section 3.1).

	Node 1	Node 2	Node 3	Node 4	Node 5	Node 6	Node 7	Node 8	Node 9
$Q_r\,[fC]$	0.3	0.6	1.0	1.3	1.6	2.0	2.3	2.8	3.2
$Q_l\,[fC]$	3.2	2.8	2.3	1.9	1.6	1.3	0.9	0.7	0.3
P	0.09	0.19	0.29	0.40	0.50	0.61	0.71	0.81	0.91
$\sigma_r = \sigma_l = \sigma_{single}\,[fC]$	0.24	0.24	0.24	0.24	0.24	0.24	0.24	0.24	0.24
σ_P	0.060	0.061	0.062	0.062	0.062	0.062	0.062	0.060	0.060

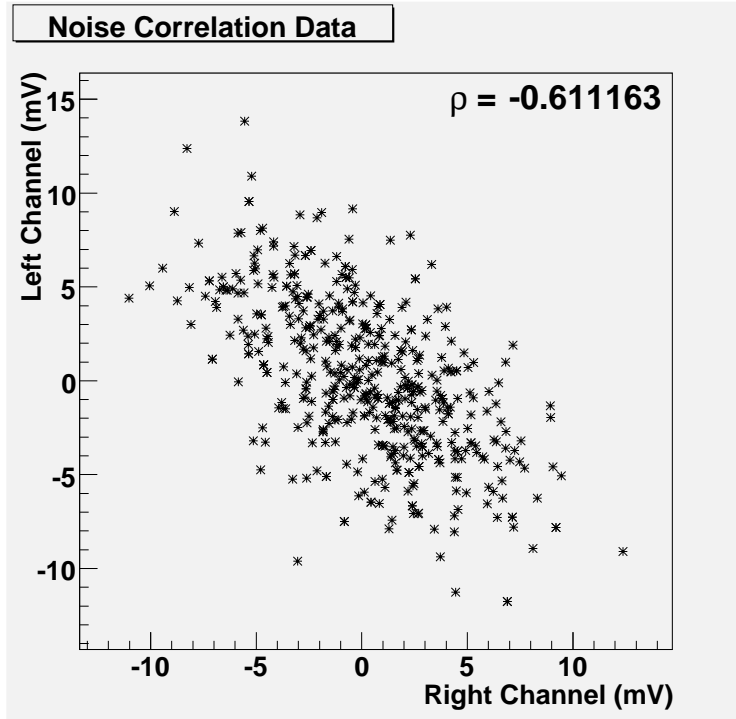Table 3.2: Signal position measurement, and corresponding resolutions, for the single-strip PC board model.

Figure 3.9: Plot of correlation measurement results using the PC board model.

3.5   Crosstalk Measurement Results

Investigation of the amount of crosstalk that occurs is necessary to determine if the five-strip model will impact the SNR. Preliminary measurements were made of the shaped output signal of the nearest and farthest neighboring strips, the results of which are shown in Figure 3.10. Noticing the significant peak amplitude of these signals, we made an initial attempt to measure the percentage of total injected charge found at the pre-amp input of the neighboring strips. This was done by measuring the current at the ends of these strips, which were terminated with a passive $6k\Omega$ resistor simulating the input impedance of the readout electronics. The current was then integrated over using the PSpice S integration command in the time domain. We found that roughly 1% of the total injected charge is seen at the pre-amp inputs of the neighboring strips. The measured current waveforms are shown in Figure 3.11. These measurements are not conclusive, however, as we did not have enough time to properly analyze the methods used, nor compare with the single-strip sensor results.
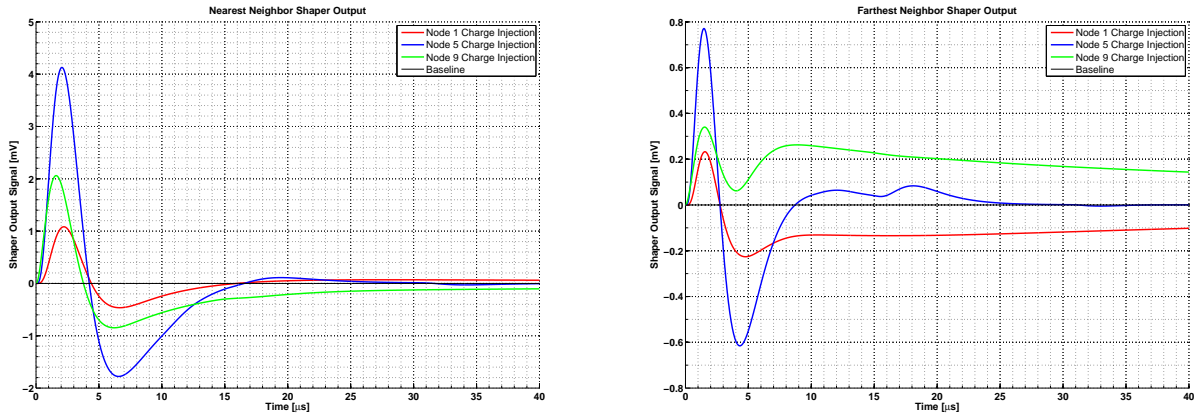
Figure 3.10: Shaped signal output of the five-strip model for the nearest and farthest strips for a charge injection at three different nodes.
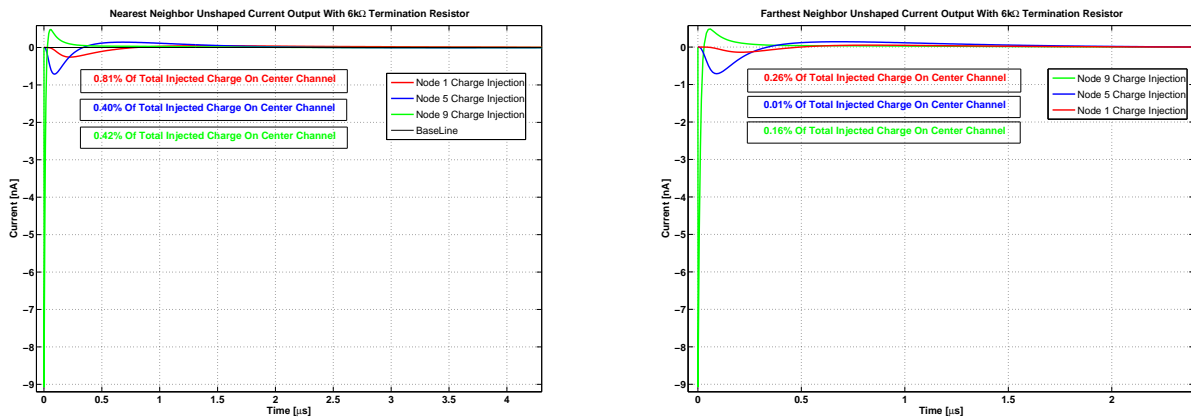

Figure 3.11: Estimated current signal at the pre-amp input of the near and far neighbor strips of the five-strip model. Results for a charge injection at three different nodes are shown. The total charge for each current waveform is also shown.

3.6 SNR Dependence On R_D And C_D

The estimates provided by the 1974 Radeka paper[8], shown by Equation 1.1, suggest the position resolution is independent of sensor resistance, and proportional to the square root of the capacitance. To investigate this, the SNR for various sensor resistances R_D and capacitances C_D were investigated. In order to do this correctly, an optimum shaping time was determined for each sensor model variation. Using the same process as outlined in Section 2.3, three total sensor resistance values of $60k\Omega$, $600k\Omega$, and $6M\Omega$ were simulated for a fixed sensor capacitance of $12.7pF$, and five total sensor capacitor values of $5.04pF$, $9.9pF$, $12.7pF$, $13.5pF$, and $18pF$ were simulated for a

fixed sensor resistance of $600k\Omega$. The readout electronics component values used for the optimum shaping setup of each model variation are shown in Table B.3.

The results of the simulation exploring dependence on sensor resistance agrees well with the prediction as shown in the right graph of Figure 3.12. Note that there is a noticeable 4% difference in the node 1 SNR between the $60k\Omega$ plot and the other two. This is likely due to the fact that the method used to determine the optimum shaping time for each setup has a $\pm5\%$ error (refer to Section 2.3).
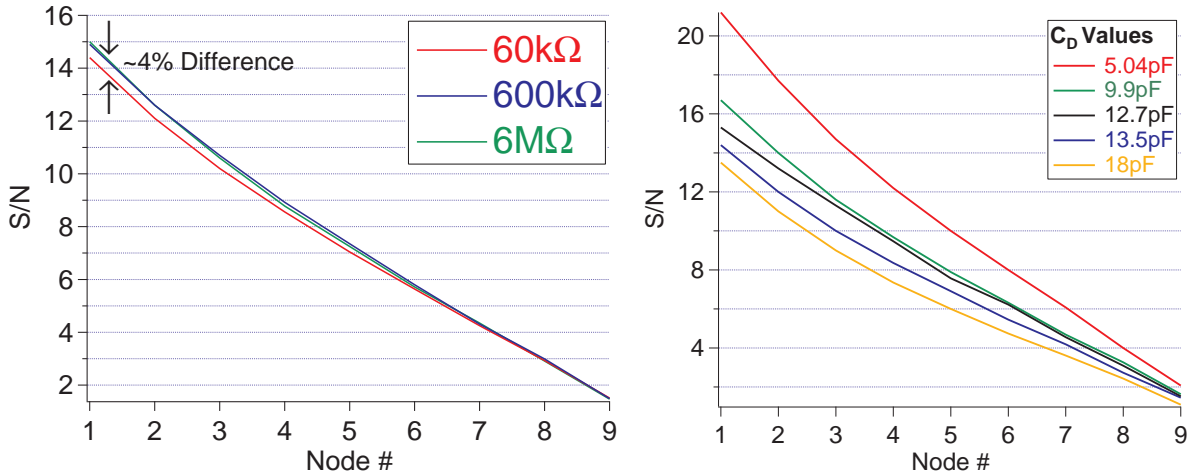

Figure 3.12: Figures showing single-strip SNR dependence on sensor resistance and capacitance. For the left figure $C_D = 12.7pF$, and for the right figure $R_D = 600k\Omega$.

The simulation investigating sensor capacitance dependence did show significant variation in SNR, the results of which are shown in Figure 3.12. However, this dependence does not agree well with the square root dependence prediction. If we assume the correlation coefficient ρ remains the same for the five-strip model, then Eqn. 3.3 shows that the fractional position resolution scales inversely with SNR. With this we can do a back-of-the-envelope calculation by taking the ratio of the square root of the two extreme sensor capacitances measured, $\sqrt{18pF}/\sqrt{5.04pF} = 1.89$, and compare

this with the ratio of the two node-1 SNR values associated with these capacitances $^{21}/_{13.8} = 1.52$. This shows that a $\sim 90\%$ decrease in SNR is predicted from the theory, whereas a $\sim 50\%$ decrease is found from the measurements shown in Figure 3.12. A possible explanation for this is variation in signal shape parameters between the different sensor capacitances explored, resulting in the γ factor in Eqn. 1.1 playing a role when looking at these ratios. Also, the correlation coefficient is likely not the same magnitude between the singe- and five-strip models. This result has not been investigated further.

Chapter 4

Conclusion

This thesis presents the first exploration of the use of resistive charge division to obtain a longitudinal position coordinate measurement using silicon strip sensors. The results demonstrate the viability of this method for reducing fake tracks within the detector volume for ILC high-energy particle collisions, thereby improving pattern recognition capability. A single-strip model of a silicon strip sensor using discrete analog components was constructed on a printed circuit board using a ten-node division of a $10cm$ long, highly resistive, silicon strip sensor with $^{60k\Omega}/_{node}$ and $^{1.39pF}/_{node}$. Readout electronics consisted of two charge sensitive pre-amps that created a virtual ground at the back ends of the strip, with the output of each pre-amp AC-coupled to a three stage integration shaper. The results of this single-strip model were used to benchmark a PSpice computer simulation to within 5%, after accounting for stray capacitances and scaling by the measured gains of the readout electronics. The single strip model was then duplicated to make a five-strip PSpice computer simulation with 40% of the $^{1.39pF}/_{node}$ capacitance coupled to ground and 60% coupled to neighboring strips.

A position measurement resolution of 6.1% of sensor length was obtained for the single-strip model, with an optimum SNR of 7.2 for a center node injection, and a readout electronics shaping time of $2.0\mu s$. For a $10cm$ long sensor, these results surpass the $\leq 1cm$ measurement resolution goal put forward by Meyer et. al.[6] for shaping times relevant to ILC beam delivery specifications. These results are also comparable with the 6.5% position resolution prediction by V. Radeka [8], which requires a longer $3.1\mu s$ shaping time. Extension of this model to five strips using the PSpice

computer simulation indicated a possible $5\% - 6\%$ reduction in the SNR for the shaping time of $2.27\mu s$. It should be noted that the low SNR of these results may impact the transverse coordinate measurement. Exploration of this effect is a necessary next step in confirming the attractiveness of this method for ILC tracking measurements.

A linear relationship between measured and actual signal position was found for the single-strip model, even with noticeable non-linearity in SNR for the $2.0\mu s$ shaping time. This argues that the $< 0.2\%$ non-linearity constraint imposed by [8] is unduly restrictive, and leads to unnecessary degradation in the longitudinal position resolution. Position measurement resolution also proved to be largely independent of signal position along the entire length of the sensor strip, showing the $2.0\mu s$ shaping time to be sufficient for the successful application of resistive charge division for the silicon sensors considered here.

Independence of SNR from sensor resistance, as predicted by [8], was verified. In addition, a strong dependence of SNR on sensor capacitance was found, although it did not agree with the square root prediction as shown in Eqn. 1.1. Investigation into an explanation was not done here. However, possible reasons include variation in shaping parameters between the different capacitances measured, and a variation in the correlation coefficient between the different models of various capacitances.

Appendix A

Layout Of The Four Printed Circuit Board Layers

Note that the PC board design actually includes an additional node that is not used. This node was included to allow the ability of AC-coupling the readout electronics on one end of the sensor model. However, it was found that AC-coupling was not necessary for this project, so this node was loaded with a 0Ω jumper. This AC-coupling node does introduce additional stray capacitance, although the effect was shown to be negligible in simulation.

Lyr	s-p	Layer Type	Thick.**	MClad	FClad	qty	Core/PP	Base	Foil
1	s		0.0007	0.5	0.5				S
			0.0060			2	1080	1	
			0.0069			1	7628	1	
2	p		0.0308	1	1		0.0280	0	S
3	p			1	1				S
			0.0069			1	7628	1	
			0.0060			2	1080	1	
4	s		0.0007	0.5	0.5				S

Figure A.1: Material cross section of the printed circuit board as claimed by the manufacturer Sierra Proto Express.

Figure A.2: Layout of the first layer of the printed circuit board.

Figure A.3: Layout of the second layer of the printed circuit board.

Figure A.4: Layout of the third layer of the printed circuit board.

Figure A.5: Layout of the fourth layer of the printed circuit board.

Appendix B

Tables Of Shaper Component Values

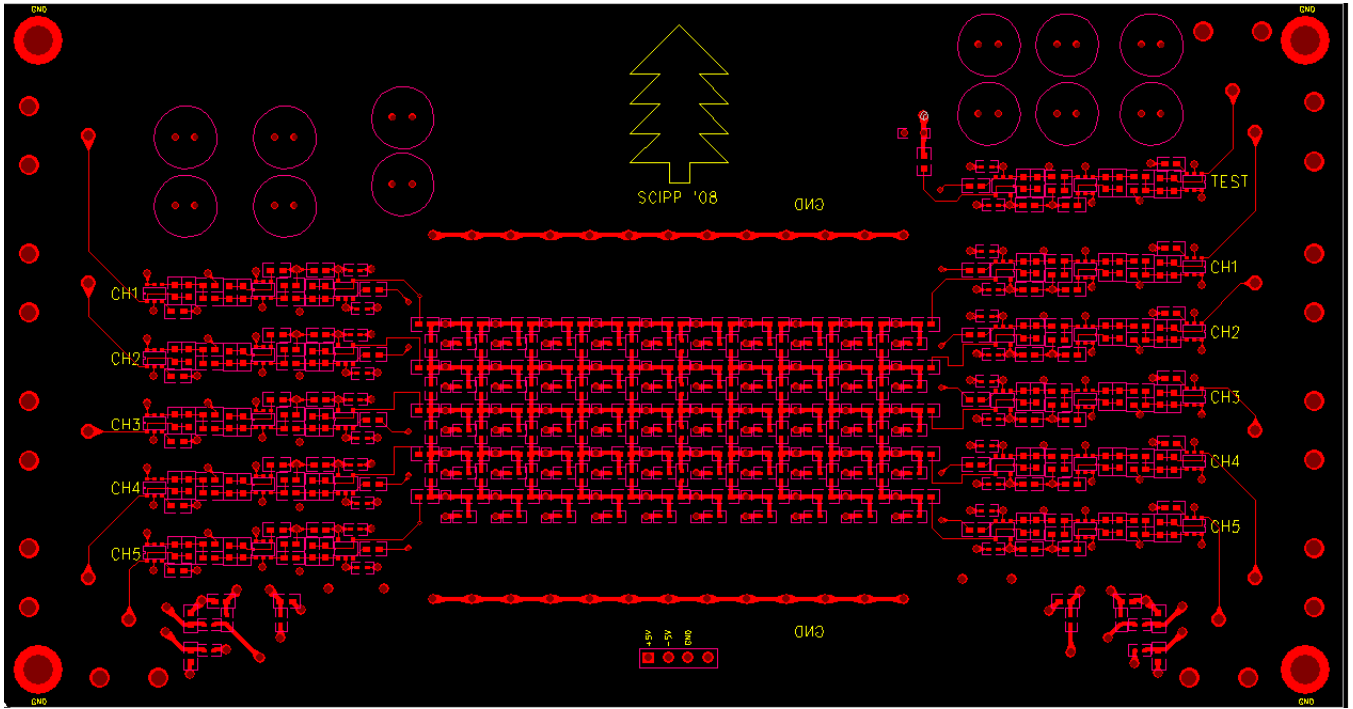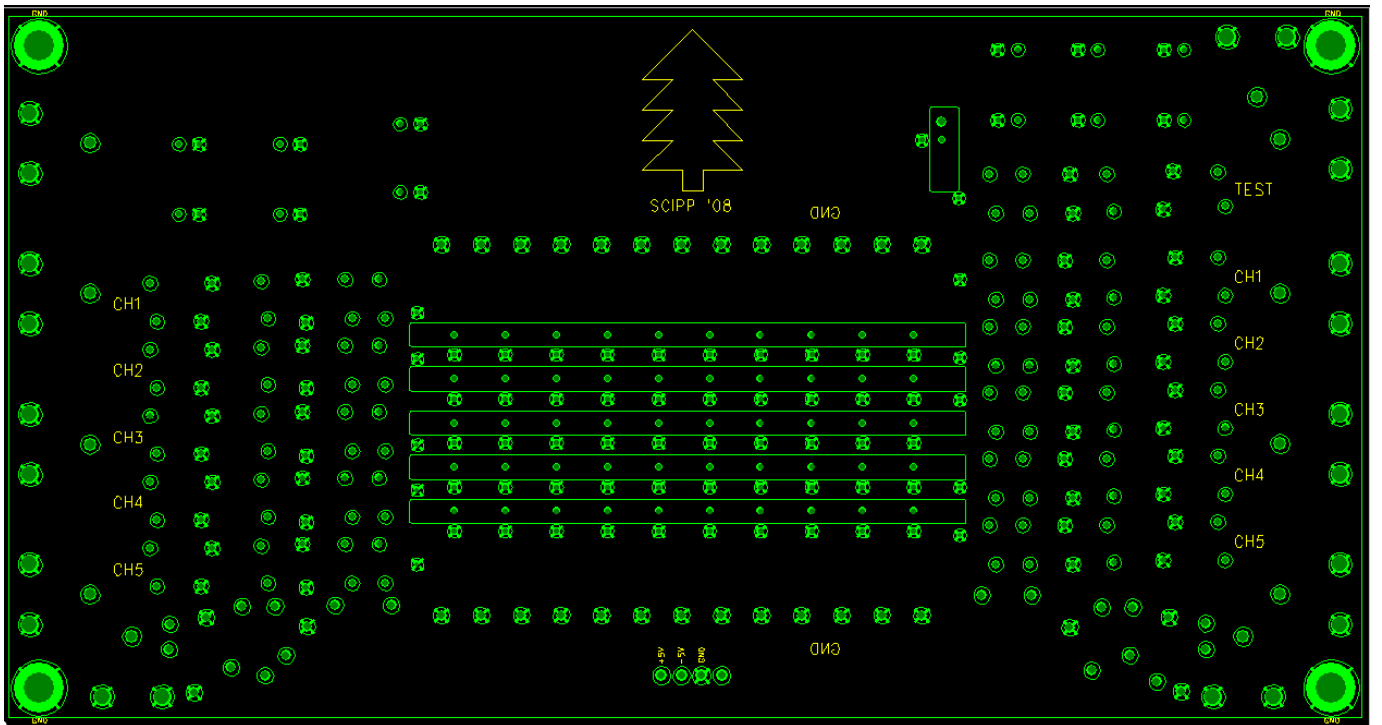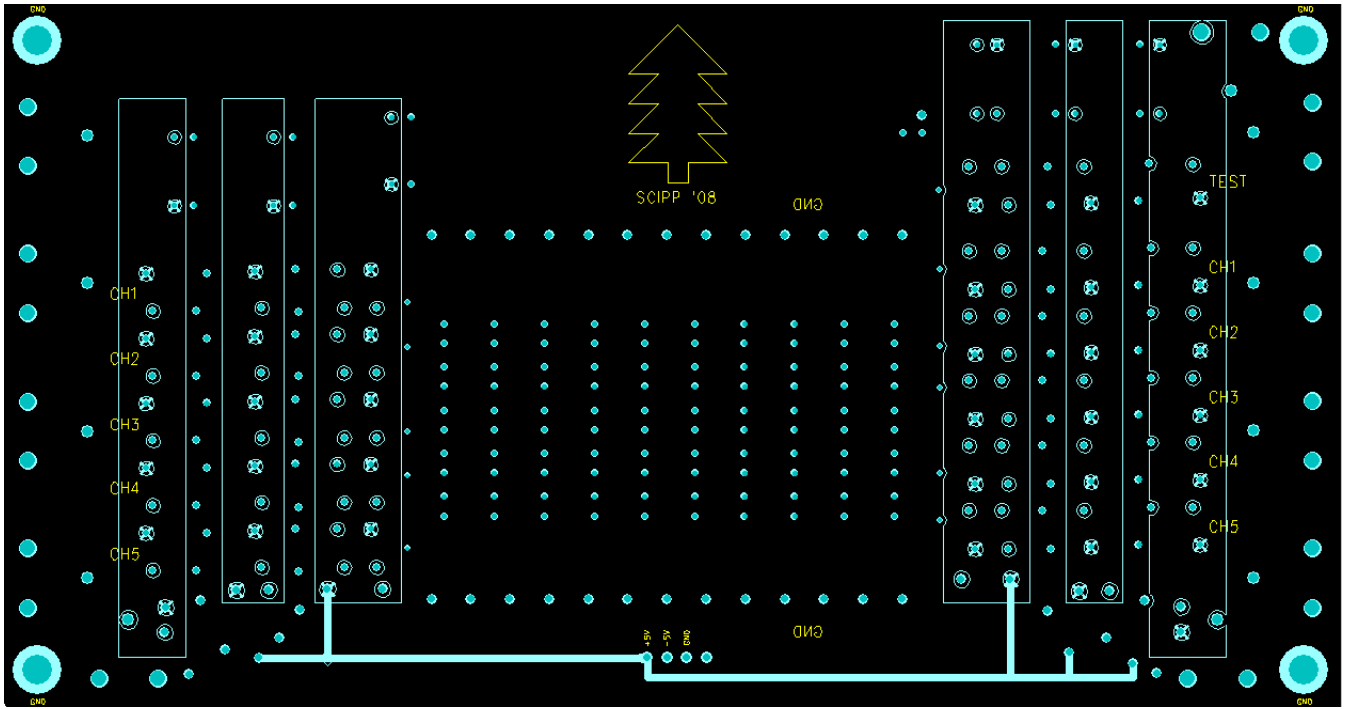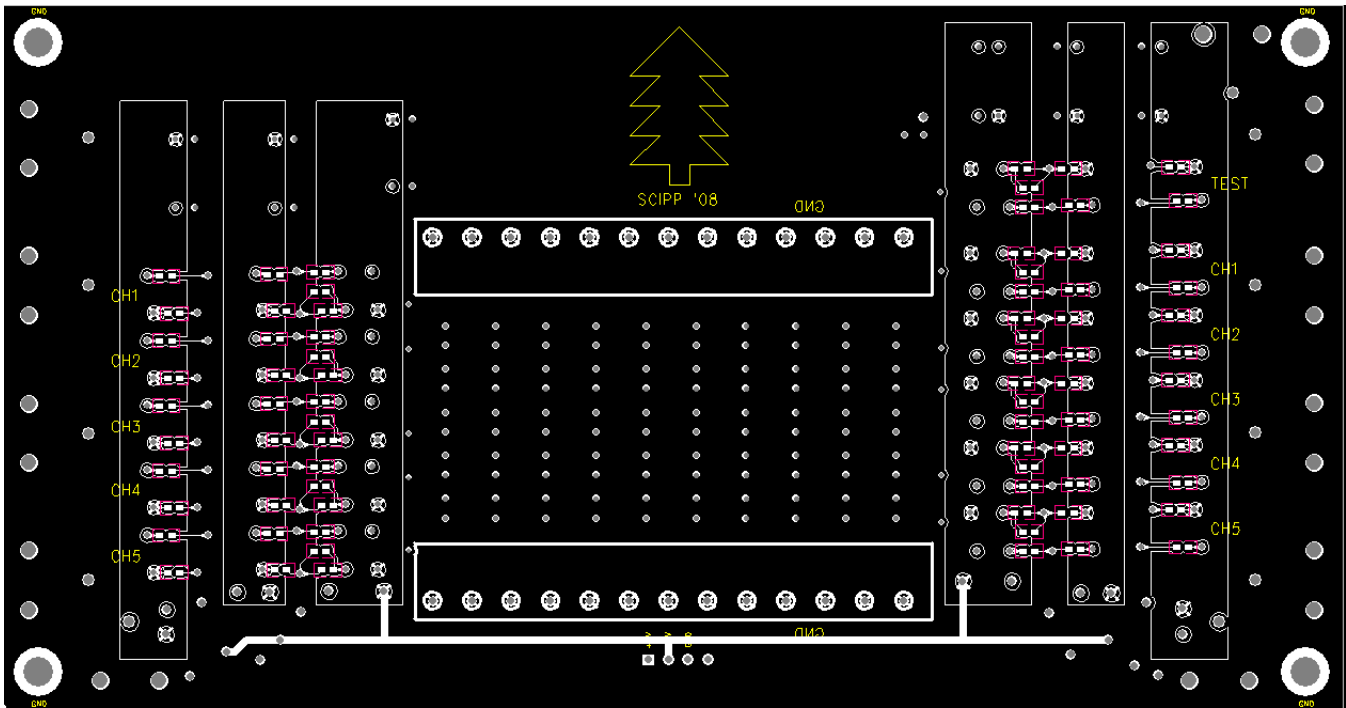| Single-Strip Model ($T = 0.80\mu s$)							
	$\frac{1}{4}T$	$\frac{1}{2}T$	$1T$	$2T$	$2.5T$	$3T$	$4T$
R_{1f}	$2.8M\Omega$	$5.65M\Omega$	$5.65M\Omega$	$5.65M\Omega$	$5.65M\Omega$	$5.65M\Omega$	$5.65M\Omega$
C_{1f}	$65fF$	$65fF$	$0.129pF$	$0.258pF$	$0.324pF$	$0.388pF$	$0.517pF$
R_d	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$
C_d	$32nF$	$32nF$	$32nF$	$32nF$	$32nF$	$32nF$	$32nF$
R_{2f}	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$
C_{2f}	$20pF$	$40pF$	$80pF$	$155pF$	$190pF$	$255pF$	$350pF$
R_{bias}	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$
R_{int}	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$
C_{int}	$16pF$	$31pF$	$65pF$	$122pF$	$155pF$	$185pF$	$240pF$
R_{buff}	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$
R_{3f}	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$
C_{3f}	$1pF$	$1.6pF$	$3.2pF$	$6.9pF$	$8.7pF$	$9.4pF$	$12.4pF$
R_t	50Ω	50Ω	50Ω	50Ω	50Ω	50Ω	50Ω

Table B.1: Readout electronics values used in the exploration of various shaping times for optimum SNR and linearity for the single-strip model. Stray capacitances were used for this sensor model.

Five-Strip Model ($T = 0.57\mu s$)						
	$1T$	$2T$	$2.5T$	$3T$	$3.5T$	$4T$
R_{1f}	$5.49M\Omega$	$5.49M\Omega$	$5.49M\Omega$	$5.49M\Omega$	$5.49M\Omega$	$5.49M\Omega$
C_{1f}	$0.105pF$	$0.203pF$	$0.257pF$	$0.285pF$	$0.355pF$	$0.4pF$
R_d	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$
C_d	$32nF$	$32nF$	$32nF$	$32nF$	$32nF$	$32nF$
R_{2f}	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$
C_{2f}	$70pF$	$120pF$	$160pF$	$200pF$	$230pF$	$290pF$
R_{bias}	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$
R_{int}	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$
C_{int}	$42pF$	$95pF$	$115pF$	$137pF$	$170pF$	$190pF$
R_{buff}	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$
R_{3f}	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$
C_{3f}	$2.6pF$	$5.25pF$	$6.5pF$	$8.0pF$	$8.6pF$	$10.2pF$
R_t	50Ω	50Ω	50Ω	50Ω	50Ω	50Ω

Table B.2: Readout electronics component values used in the exploration of various shaping times for optimum SNR and linearity for the five-strip model. Stray capacitances were used for this sensor model.

	R_D Dependence ($C_D = 12.7pF$)			C_D Dependence ($R_D = 600k\Omega$)			
	$60k\Omega$	$600k\Omega$	$6M\Omega$	$5.04pF$	$12.7pF$	$13.8pF$	$18pF$
R_{1f}	$1M\Omega$	$5.65M\Omega$	$29M\Omega$	$2M\Omega$	$5.65M\Omega$	$5.3M\Omega$	$7.1M\Omega$
C_{1f}	$0.167pF$	$0.324pF$	$0.5pF$	$0.324pF$	$0.324pF$	$0.324pF$	$0.324pF$
R_d	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$
C_d	$32nF$	$32nF$	$192nF$	$32nF$	$32nF$	$32nF$	$32nF$
R_{2f}	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$	$2.04k\Omega$
C_{2f}	$15.5pF$	$190pF$	$2.5nF$	$80pF$	$190pF$	$185pF$	$200pF$
R_{bias}	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$	$1.02k\Omega$
R_{int}	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$
C_{int}	$14pF$	$155pF$	$1.38nF$	$60pF$	$155pF$	$145pF$	$150pF$
R_{buff}	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$	$6.2k\Omega$
R_{3f}	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$	$62k\Omega$
C_{3f}	$0.8pF$	$8.7pF$	$82pF$	$3.5pF$	$8.7pF$	$9.2pF$	$8.2pF$
R_t	50Ω	50Ω	50Ω	50Ω	50Ω	50Ω	50Ω

Table B.3: Readout electronics component values used for investigation of SNR dependence on sensor strip resistance and capacitance. These values are for the single-strip model.

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